NOVEL DIGITAL STRUCTURES UTILIZING SINGLE ELECTRON DEVICES

by

Hossam Aly Hassan Fahmy

A Thesis Submitted to the
Faculty of Engineering at Cairo University
in Partial Fulfillment of the
Requirements for the Degree of
MASTER OF SCIENCE
in
ELECTRONICS AND COMMUNICATIONS

FACULTY OF ENGINEERING, CAIRO UNIVERSITY
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Under the Supervision of

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Acknowledgments

This thesis would have not been accomplished without the great help I got from many persons. I thank my supervisors Prof. Mostafa S. Metwally and Prof. Aly E. Salama for the stimulating discussions, the attentive reading of the many drafts and the corrections made to improve the presented work.

I am specially grateful to Dr. Khalid Ismail for his invaluable guidance and encouragement. He introduced me to the field of Single Electronics and answered millions of questions with great patience. He also arranged a joint study program on single electronics between Cairo University and IBM T.J. Watson research center. The 'nano-devices' group at IBM gave me the chance to acquire a large amount of information specially on the fabrication.

I thank my father for correcting my numerous spelling and style mistakes. I am also indebted to the rest of my family and all my friends for keeping my morals high in moments where desperation seemed to be the only choice.

Finally, I would like to express my gratitude to all the persons who write and promote free software. This thesis is typeset using LaTeX, spell checked using *ispell* both running under the *Linux* operating system which are all free; the simulation software used is also free. Being independent of commercial monsters is great, freedom is priceless!!

Abstract

During the last decade the field of single electron devices has matured from pure theoretical ideas of elements working at very low temperatures (milli Kelvin range) to fabricated devices operating at room temperature. These ideas are moving now from the experimental physics to the electronic circuits domain. New applications are sought and single electron devices may become a replacement for standard CMOS in several areas.

This thesis presents a possible approach to this goal. A brief introduction of the aspects and general problems of current digital logic devices and a detailed background on single electronics theory and applications are presented. The fabrication issues of nanometer scale structures are discussed followed by a brief account on the estimation of electric parameters of such devices.

A novel multi-valued adder circuit is introduced, where the emphasis is on its implementation for decimal addition. A detailed analysis and simulation results indicating its sensitivity to different parameters are given to validate its operation. Then, a set of operators for decimal logic is built based on the adder and it is shown that it forms a complete set of logic capable of performing any decimal function. Another possible implementation of the decimal adder is also investigated. Propositions for future work are outlined.

Contents

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List of Symbols and Abbreviations

Γ	Tunneling rate
C_1, C_2, C_s, C_d	Junction capacitance
C_g, C_0	Gate capacitance
C_t, C_{tt}	Total capacitance
E_c	Charging energy
f	Frequency
h	Planck's constant
k_B	Boltzmann constant
n	Number of electrons
Q_p	Polarization charge
q	Electronic charge (positive)
T	Absolute temperature

2DEG	Two Dimensional Electron Gas
AFM	Atomic Force Microscope
CCD	Charge-Coupled Devices
CMOS	Complementary Metal Oxide Semiconductor
HBT	Hetero-junction Bipolar Transistor
HEMT	High Electron Mobility Transistor
MESFET	Metal-Semiconductor Field Effect Transistor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MVL	Multi-Valued Logic
Q-dot	Quantum dot
SECO process	Step Edge Cut Off process
SEL	Single Electron Logic
SET	Single Electron Transistor
SIMOX wafer	Separation by IMplanted OXygen wafer
STM	Scanning Tunneling Microscope

Chapter 1

Introduction

Single electronics and nano-fabrication techniques are new and growing fields in the electronics industry. This industry is currently facing a lot of challenge and problems which these technologies give the hope to circumvent. In order to appreciate this challenge and to introduce the single electronics, a discussion of the ideal characteristics required in digital logic devices is needed. Then, in view of these characteristics, different devices are evaluated in order to show the difficulties facing the current technologies and the reasons why single electronics and nano-fabrication are essential to study. The rest of this chapter discusses these two main issues. In chapter 2 the single electronics theory and its applications are presented. Chapter 3 introduces some of the nano-fabrication techniques. The new decimal adder is explained in details in chapter 4 and its use to achieve a complete set for multi-valued decimal logic is shown in chapter 5. Another implementation for the decimal adder is described and analyzed in chapter 6 and the general conclusions are given in chapter 7. Appendix A describes the simulation software used while appendix B introduces further ideas that may be explored in the future.

1.1 Ideal characteristics of digital logic devices

In this section, the suitability of a device to digital circuits is discussed according to the specifications given by Keyes [1, 2] and Landauer [3] for logic devices and according to fabrication restrictions imposed by the different technologies.

According to Keyes the devices used to handle digital signals should have the following characteristics,

At a device level:

1. In digital computations the information is iterated and the logic depth in each iteration is usually large. If the signals are allowed to deteriorate when passed from one logic element to the next the information will be completely lost within few iterations. Signal restoration is needed in order to maintain standard values for the output of the device. This means that the input/output response must be a nonlinear curve where the output is insensitive to deviations in the logic levels of the input.

2. The device should allow a fan-in (multiple sources) and a fan-out (more than one device connected to its output) without deteriorating the signal levels. This usually means that the device must have a voltage or current gain.

3. The output must be isolated from the input of the device so that it would not affect the input levels. The signal propagation must be unidirectional or the overall system may not function correctly.

4. To have a complete logic set there must be a way to invert the signals. Even if this is not available directly by the device, alternative methods like threshold logic [1] can be used (although the performance may suffer according to that.)

As for the overall system environment:

5. In current circuits the number of components on the chip is on the order of millions. The cost as well as the power consumed per component must be as low as possible. These two factors, the cost and the power dissipation (as well as other technological factors sometimes), hinder the use of several proposed devices.

6. Since the number of components is high the reliability of each individual device must be very high otherwise the lifetime of the system will be relatively short.

7. Technology related parameters are difficult to control and often have a wide range of tolerances. The designers must accept this reality and circuits must operate in the presence of deviations in device characteristics from standards. The situation may be even aggravated by stressing or aging of the components. This means that devices must have high gains to enable them to perform adequately in the computer environment. The high gain is suitable also to allow fan-out as discussed above since the device usually controls voltages and currents larger than those needed to operate it.

8. If the device needs a separate resetting after each operation performed, the wiring needed increases and the system performance may degrade. Simple wiring schemes should always be sought.

9. To get a fast computer system, not only fast devices are needed but also the distances and the transit times of the signals on the connections between the devices must be considered. Devices cannot be packed close together beyond some limits which are set either by the technology used or by the power dissipation and the heat removal capacity of the system.

Two more points were addressed by Landauer [3]:

10. Miniaturization has its own problems. While speaking about molecular electronics, Landauer asks "How do we make effective and reliable contact with such small entities?" This in fact applies also to all the new nano-scale semiconductor devices.

11. While presenting the logic based on the nonlinear electro-magnetic interactions Landauer says "No scheme which requires precisely-timed signals at every stage has been truly successful". Simple clocking schemes should always be used. Although it is about complex timing schemes proposed for some digital circuits this argument may also emphasize the need for simple wiring schemes mentioned in 8 above.

The above eleven points may be met to varying degrees in any proposed technology but they must be observed when comparing different proposals for implementation.

1.2 Traditional devices

The history of digital logic has been marked by the use of several devices meeting to different degrees the requirements mentioned above.

The first device used in modern computers was the relay. The relay is nearly a perfect digital device except for the facts that its failure rate is high, its heat dissipation is also high, it has a big size and its speed is quite slow due to its mechanical action [2]. Vacuum tubes alleviated the last problem (speed) by eliminating the mechanical switching of the device and the first digital computers became a reality. Then came the semiconductors era.

The semiconductor digital circuits began with the Resistor Diode Logic (RDL) which was smaller in size, faster and with less power dissipation but compromised to some extent the I/O isolation. They were soon replaced by the Resistor-Transistor Logic (RTL) which had a good I/O isolation but which consumed a lot of semiconductor area when fabricated on a single chip due to the large resistances. This paved the way to the Transistor-Transistor Logic (TTL) based on the bipolar transistor and the Complementary-Metal-Oxide-Semiconductor (CMOS) based on the use of a pair of complementary MOSFETs one of the N-type and one of the P-type.

The Bipolar-Junction Transistor (BJT) and its logic families have been replaced in a lot of applications by the CMOS due to its lower power dissipation and small area. As the CMOS is scaled down to smaller sizes its area and power dissipation decrease while its speed increases. This is the reason why it became the "state of the art" device for digital micro-electronics nowadays with its ideal characteristics fulfilling, to a good degree, all the points of an ideal logic device.

1.3 Non-traditional devices

The quest for higher speed, lower power dissipation and smaller area remains thus the main drive for improving on the current devices. The improvements are sought through two parallel ways: the materials study and the introduction of new devices.

1.3.1 Different semiconductor materials

The semiconductor material mainly used is silicon. This is due to some electrical characteristics as well as its low cost, availability and advanced fabrication technologies. A comparison with Germanium and Gallium Arsenide was presented by Keyes [1]. Germanium has a higher electron and hole mobilities than silicon which leads to a faster operation. However, germanium oxide does not have the good dielectric qualities of silicon dioxide nor its excellent chemical properties. Also germanium has a narrow energy gap compared to silicon. With a large number of devices per chip and the increase in temperature, electrons can be excited across the intrinsic energy gap and proper operation may not be maintained. Even before this happens, the small energy gap results in larger junction leakage which increases the power dissipation. The compound material of silicon and germanium, SiGe, may prove to be a better candidate specially with the introduction of new device ideas [4].

Gallium Arsenide (GaAs) has proved its usefulness in special areas due to its inherent characteristics. The electron mobility in GaAs is much higher than in silicon but the hole mobility is lower. This leads to the fact that no complementary logic is fabricated using GaAs which in turn leads to a higher power dissipation. The properties of other compound semiconductors like Indium Phosphide and Aluminum Arsenide are comparable to those of GaAs in the fact that there are no complementary devices and that usually the electron mobility is higher than in silicon. These materials are however more suitable to optical applications since they have a direct energy band gap which is equivalent to energies of photons in the visible range of light.

Due to these special characteristics of the compound semiconductors, their use was mainly restricted to certain devices like the Metal-Semiconductor FET (MESFET), the High Electron Mobility Transistor (HEMT), and the Hetero-junction Bipolar Transistor (HBT) where the emphasis is on the speed of operation for microwave applications. Light emitting and detecting devices constitute another area of application for these materials. Till now, and mainly because of the high power dissipation and technological difficulties, the compound semiconductors have not been widely used for digital applications.

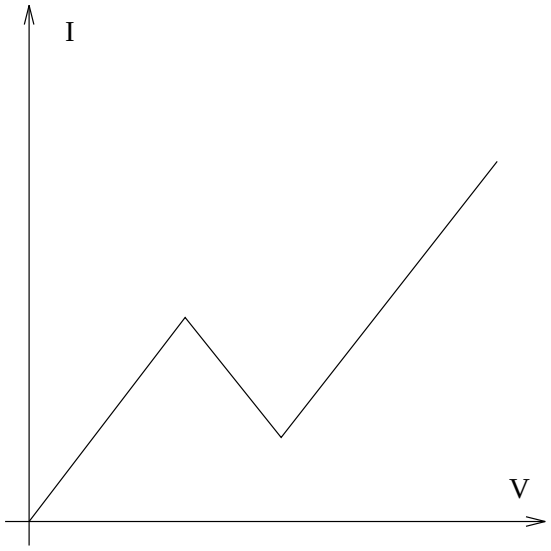

Figure 1.1: I-V characteristics of a tunnel diode.

1.3.2 Device ideas

As for new device ideas, several devices were proposed to perform digital logic. Tunneling devices and Gunn diodes have been the first candidates. Due to the negative differential resistance characterizing the I-V curve of these devices (Fig. 1.1), several application ideas were introduced.

Resonant tunneling diodes are two terminals devices which were proposed for digital logic implementation by several research groups [5, 6]. However, since they only posses two terminals, input/output isolation in the circuits using them is compromised. This problem was relaxed by the use of resonant tunneling transistors in the circuits of Mohan *et al.* [7, 8]. But still according to the points mentioned in section 1.1 there are some major problems left unsolved.

Separate resetting is needed, the gain of each element is not large enough and the implementation of inversion is not straight forward. Another problem is that the off-state of these devices is not really zero resulting in "power-hungry" circuits. Besides all this, the dependency of this technology on accurate device parameters is essential. This is explained by Keyes [2] and he shows the limitations of such dependency.

The technology has its own implementation problems. As reported in the analysis remarks of Arafa [9] on the fabrication of tunneling devices "A more rigorous study of the effect of the technological parameters needs to be conducted. The

absence of the assumed depletion region near the surface resulted in a short circuit current that masked all NDC [Negative Differential Conductance] characteristics." So, fabricated devices may not work after all!

Another minor problem that faced the researchers was the absence of good simulation models for such devices but this can be easily overcome as new models appear [10].

Resonant tunneling structures seem thus to violate the majority of the requirements of a good digital device. They may be used for some specific applications but in view of the current technology they are not yet suited for digital logic.

Another class of non traditional devices is the superconducting Josephson junctions. Keyes [2] discussed their use for digital logic and concluded that they present mainly the same problems as those of the tunneling devices. They also have the disadvantage of requiring a low temperature for operation (few degrees Kelvin) which leads to a high cost for the heat removal from the system.

1.4 Current status of the technology

CMOS technology is the current "state of the art" for the majority of electronic applications. This fact is due to its complementary characteristics, and mature technology. However, improvements are needed: higher speed and higher packing density for the devices per chip, while not exceeding the power dissipation limits. These factors are not independent of each other. Considering only dissipative systems (non-dissipative systems will be discussed later), one can derive a relation for the dynamic power that must be removed from the chip package (P_d) in terms of the frequency of operation (f), the absolute temperature (T), the number of devices per chip (N) and the number of electrons transferred in a single switching event of a transistor (n) [11]. Assuming that, in order to transfer a single electron, the device consumes an amount of energy per switching event just equal to the thermal energy k_BT where k_B is Boltzmann constant (usually in current devices it is much more than that) then we find that the above quantities are related by:

$$P_d = aN \times n(k_BT) \times f \tag{1.1}$$

where a is the percentage of devices activated in a clock cycle which varies depending on the design and ultimately we can assume it to be one.

It is thus clear that to increase the packing density, by increasing N, while keeping a small power dissipation and the same frequency, n must decrease. This has been the trend for the past few years. By scaling down the device size, a larger N can be used but at a smaller current density out of the device. The small size helps to keep the input capacitances of the cascaded devices small which means that the frequency of operation is not greatly affected by the poor current driving capability.

This scaling down is not without end. If it comes to the transfer of a single electron or the size is at the atomic level no more scaling can be done. This is why the study of the field of single electronics is of importance today: it promises to be the solution for tomorrow.

Chapter 2

Background to Single Electronics

2.1 Basic idea of single electronics

To explain the basic idea of single electron devices consider the structure shown in Fig. 2.1(a). It represents two metallic electrodes, the source and drain, and between them a third metallic 'island' surrounded by an insulating material. If the thickness of the insulator between the island and the electrodes is small enough, electrons may tunnel through when an external bias is forced on the source and drain contacts. The equivalent circuit of this device is as shown in Fig. 2.1(b).

Electrons can acquire enough energy to tunnel either from the external bias or from the thermal agitation energy, k_BT, where k_B is Boltzmann constant and T is the absolute temperature. To have a controlled transfer of electrons, the required charging energy must be greater than k_BT. This energy is the one needed to charge the capacitances associated with the island. By controlling the value of the total capacitance of the island, C_t, the energy needed to charge it by a single electron, $E_c = q^2/(2C_t)$, is made larger than k_BT. Depending on the size of the island, its capacitances to the source, C_s, and drain, C_d, can be made as small as needed which leads to a smaller total capacitance $C_t = C_s + C_d$, hence a higher charging energy. Also, if C_t is small the variation of the island potential due to this single charge transfer (q/C_t) is considerable.

The key point is that if the capacitances are small, leading to $E_c \gg k_BT$, then the transfer of a single electron can be achieved in a controlled manner and can be easily detected. However, this is not the only condition. For each tunnel

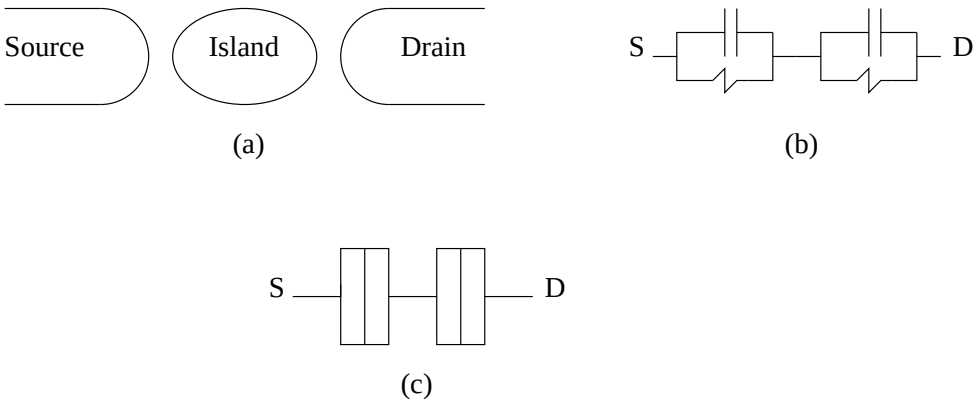

Figure 2.1: The basic single electron transistor.
(a) A small conducting island between two electrodes.
(b) Its equivalent circuit.
(c) the conventional circuit schematic used for tunnel junctions.

junction, the energy uncertainty associated with the time constant of tunneling $\tau = R_T C$ must be less than E_c[1]. This necessitates that the tunneling resistance, R_T, must be much greater than the resistance quantum $R_K = h/q^2 \approx 25.8k\Omega$. This condition essentially insures that the wave function of the excess electron on the island is localized there [12]. In the limit when $R_T \gg R_K$, a quasi-classical theory, the 'orthodox' theory, for single electronics was derived by Averin and Likharev [13, 14]. The theory implies that the rate of tunneling events is given by

$$\Gamma = \frac{I((\Delta E)/q)}{q(1 - \exp(-\frac{\Delta E}{k_B T}))} \tag{2.1}$$

where ΔE is the decrease in potential energy due to the tunneling event. At low temperatures, $k_B T \ll \mid \Delta E \mid$, the rate Γ nearly vanishes for $\Delta E < 0$, i.e. when the tunneling event increases the energy. The intuitive rule of thumb is thus: *A tunneling event occurs as soon as it decreases the potential energy of the system.* Although the majority of the work in the single electronics field concentrates on the limit where the thermal energy is much smaller than the charging energy, it is important to note however that the opposite limit has been also investigated. When $k_B T \gg E_c$, one dimensional arrays of tunnel junctions exhibit features suitable for primary thermometry. Absolute temperature can be deduced from the conductance characteristics of the array [15]. In the next section, a simple

[1]The Heisenberg uncertainty principle gives: $\Delta E \Delta t \sim h$.

derivation for the rate equation and the I-V characteristics is presented using the same steps followed by Tucker [16].

2.2 Mathematical relations and I-V curves

In order to investigate the equations governing the behavior of a voltage biased double junction structure (Fig. 2.1), the current biased single junction must be explained first. Then, based on this explanation, the relations of the double junction device and hence the Single Electron Transistor (SET) can be derived.

2.2.1 Current biased single junction

Fig. 2.2 illustrates an isolated tunnel junction having a capacitance C and tunnel resistance R and which is biased by a current source I. Similar to what Tucker did [16], the elemental charge q is considered here to be positive and the direction indicated by the arrow to be the forward direction and hence is designated hereafter by a (+) sign. Let n represent the net number of electrons that tunneled through the junction, then $n = n_+ - n_-$, i.e. it is the difference between the number of forward and reverse tunneling events. According to these definitions, the charge Q on the junction capacitance is given by

$$Q = \int_{-\infty}^{t} I\,dt - nq \tag{2.2}$$

Q is incremented *continuously* by I, but decreases in a *discrete* manner through tunneling of electronic charges. The occurrence of a forward tunneling event causes the transition $Q \to Q - q$ which is accompanied by a change in electrostatic energy equal to

$$\Delta E^+ = \frac{Q^2}{2C} - \frac{(Q-q)^2}{2C} = q\frac{Q}{C} - \frac{q^2}{2C} \tag{2.3}$$

This energy is exchanged for an increase of the electron free energy as it tunnels in the forward direction. It is seen that the first term is q times the junction voltage V defined as $V = Q/C$ (note that Q is a function of n so this relation can be actually written as $V(n) = Q(n)/C$). For $V < q/(2C)$ (or $Q < q/2$), the final state has a higher energy than the initial state ($\Delta E^+ < 0$) and it is clear that no

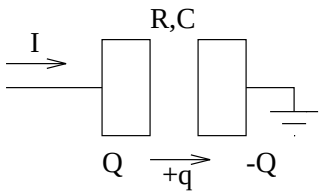

Figure 2.2: Current biased single junction.

forward tunneling can occur in this range for the low temperature limit $T \to 0$.

Similarly, tunneling in the reverse direction causes the transition $Q \to Q + q$ having an energy change of

$$\Delta E^- = \frac{Q^2}{2C} - \frac{(Q+q)^2}{2C} = -q\frac{Q}{C} - \frac{q^2}{2C} \tag{2.4}$$

Here, the final state has a higher energy for $V > -q/(2C)$ (or $Q > -q/2$). It is thus seen that, for the range $-q/(2C) < V < q/(2C)$, tunneling is suppressed in both directions for the low temperature limit. Beyond these limits, tunneling occurs and the current will follow the same curve representing the DC I-V characteristics of the junction (linear with the slope of $1/R$) but shifted to this new starting point. Actually the ordinary DC I-V curve can be obtained by measuring the current when this junction is voltage biased. A voltage source V maintains the charge $Q(= CV)$ constant on the junction and compensates for the fluctuations caused by the tunneling events. This means that the electrostatic energy will be restored to its original value after the tunneling event, and there will not be any range where this energy is negative. In other words, there exists no range of voltages where the tunneling is suppressed even at temperatures approaching zero. At higher temperatures, the ratio of the reverse and forward components of the current is given by the Boltzmann factor, $\exp(-qV/k_BT)$ [16], so that

$$I(V) = I^+(V) - I^-(V) = I^+(V)(1 - \exp(-qV/k_BT)) \tag{2.5}$$

$$I^+(V) = \frac{I(V)}{1 - \exp(-qV/k_BT)} \tag{2.6}$$

$$I^-(V) = \frac{I(V)\exp(-qV/k_BT)}{1 - \exp(-qV/k_BT)} \tag{2.7}$$

In the current biased junction and because of the shift to the new starting points mentioned above, one finds that the forward direction current is $I^+(V - q/(2C))$

and the reverse direction current is $I^-(V + q/(2C))$. *The measured voltage at a certain current bias is not equal to the voltage bias required to drive the same current but is shifted by* $q/(2C)$. These starting points can be defined as the effective voltage for the tunneling event to occur, and they are also equal to the *decrease* of the electrostatic energy (divided by q) due to the tunneling event.

$$V^+ = V - q/(2C) = (\Delta E^+)/q \tag{2.8}$$

$$V^- = V + q/(2C) = (-\Delta E^-)/q \tag{2.9}$$

Note that for V^-, $(-\Delta E^-)$ is used since this is what gives the *decrease* in energy. The tunneling rates are thus given by

$$\Gamma^{\pm} = \frac{I^{\pm}(V \mp q/(2C))}{q} \tag{2.10}$$

which for the forward direction simplifies to

$$\Gamma^+ = \frac{I(V^+)}{q(1 - \exp(-qV^+/k_BT))} \tag{2.11}$$

This is, basically, the same as equation 2.1.

According to this discussion $V(n) = Q(n)/C$ is increased by the current following the relation $V(n) = (\int_{-\infty}^{t} I\,dt - nq)/C$ and no tunneling events occur till it reaches $q/(2C)$. At this point, an electron tunnels and reduces V to a value of $\approx -q/(2C)$ and it starts to increase again to reach the point $q/(2C)$ where the tunneling is repeated. This process will thus occur with a frequency $f_{SET} = I/q$. This oscillation frequency of the voltage when the device is current biased occurs also for double and multi junctions devices.

For further discussion on the I-V curve of the current biased single junction, the reader is referred to Tucker's paper [16].

2.2.2 Double junction and SET

Fig. 2.3 illustrates a voltage biased double junction with a capacitive coupling to the central electrode. External voltage sources, V and U, are applied to the electrode of junction 1 and to the capacitor connected to the central electrode.

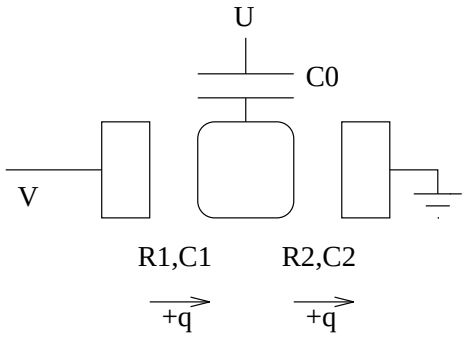

Figure 2.3: Voltage biased double junction.

The relation governing the voltages is $V = V_1 + V_2$, where V_1 and V_2 are the potential differences on junction 1 and 2 respectively. The charges associated with each of the capacitors shown in the figure are thus

$$\begin{aligned} Q_1 &= C_1 V_1 = C_1(V - V_2) \\ Q_2 &= C_2 V_2 \\ Q_0 &= C_0(U - V_2) \end{aligned} \tag{2.12}$$

The charge Q on the center island is then given by $Q = Q_2 - Q_1 - Q_0 = Nq + Q_p$ where $N = n_1 - n_2$ is the number of excess electrons present on the island and Q_p is the background polarization charge due to any impurities in the oxide barriers or any differences of the work functions between the electrodes. By defining the total island capacitance as $C_t = C_0 + C_1 + C_2$ and combining the above equations to solve for V_1 and V_2 one gets

$$V_2(N) = \frac{C_1 V + C_0 U + Nq + Q_p}{C_t} \tag{2.13}$$

$$V_1(N) = \frac{(C_0 + C_2)V - C_0 U - Nq - Q_p}{C_t} \tag{2.14}$$

The electrostatic energy of the double junction capacitors is

$$\begin{aligned} E_{total} &= \frac{Q_0^2}{2C_0} + \frac{Q_1^2}{2C_1} + \frac{Q_2^2}{2C_2} \\ &= \frac{1}{2}C_0(U - V_2)^2 + \frac{1}{2}C_1(V - V_2)^2 + \frac{1}{2}C_2 V_2^2 \end{aligned} \tag{2.15}$$

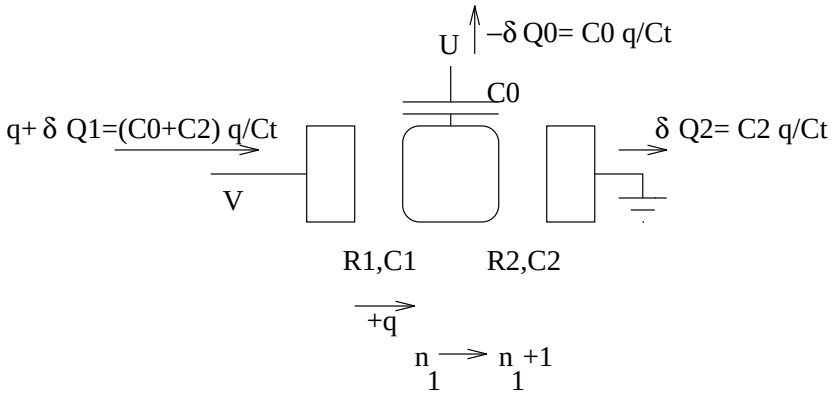

Figure 2.4: Charge transfers due to a single electron tunneling.

Using simple algebraic substitutions, this formula can be transformed to give the energy in terms of the external voltages and the island charge as follows

$$E_{total} = \frac{1}{2}C_1V^2 + \frac{1}{2}C_0U^2 - \frac{(C_1V + C_0U)^2}{2C_t} + \frac{Q^2}{2C_t} \tag{2.16}$$

Note that only the last term in this equation is affected when an electron tunnels in or out of the island. The others are constants specified by the external potentials. This total energy is equal to the sum of the stored energy in the capacitors and the work done by the voltage sources for electrons to tunnel. In fact, consider the case of one electron tunneling through junction 1 in the forward direction. This produces the transitions $n_1 \rightarrow n_1 + 1$, $\delta Q = q$ and $\delta V_2 = q/C_t$.

Inserting these values in equation 2.12 leads to the required charge transfers shown in Fig. 2.4. So the work done by the external voltage sources during tunneling events across junction 1 is estimated as

$$W(n_1) = n_1(\frac{C_0 + C_2}{C_t}qV - \frac{C_0}{C_t}qU) \tag{2.17}$$

A similar analysis for junction 2 produces,

$$W(n_2) = n_2(\frac{C_1}{C_t}qV + \frac{C_0}{C_t}qU) \tag{2.18}$$

The stored energy in the capacitors can now be estimated by combining all the above results.

$$\begin{aligned} E(n_1,n_2) &= E_{total} - (W(n_1)+W(n_2)) \\ &= \frac{Q^2}{2C_t} - \frac{n_1 q}{C_t}((C_0+C_2)V - C_0U) \\ &\quad - \frac{n_2 q}{C_t}(C_1V + C_0U) + \cdots \end{aligned} \tag{2.19}$$

As before, the difference of this energy value during a tunneling event represents the change of this electron free energy. For the forward and reverse directions tunneling across junction 1, this difference is

$$\begin{aligned} \Delta E_1^{\pm}(n_1,n_2) &= E(n_1,n_2) - E(n_1 \pm 1, n_2) \\ &= \mp\frac{qQ}{C_t} - \frac{q^2}{2C_t} \pm \frac{q}{C_t}((C_0+C_2)V - C_0U) \\ &= -\frac{q^2}{2C_t} \pm qV_1(N) \end{aligned} \tag{2.20}$$

The last result is obtained by using equation 2.14 for $V_1(N)$. Similarly, for junction 2 one finds

$$\Delta E_2^{\pm}(n_1,n_2) = -\frac{q^2}{2C_t} \pm qV_2(N) \tag{2.21}$$

These results indicate that, similar to the single junction, the effective voltages for forward and reverse directions are defined for the two junctions by

$$V_{1,2}^{\pm} = V_{1,2}(N) \mp \frac{q}{2C_t} \tag{2.22}$$

giving the following tunneling rates for the individual junctions,

$$\Gamma_{1,2}^{\pm}(N) = \frac{I_{1,2}^{\pm}(V_{1,2}^{\pm})}{q} \tag{2.23}$$

The forward and reverse current components are given by the DC characteristics of the two junctions according to equations 2.6 and 2.7.

As a simple application of the derived results, consider the case when $U = 0$, $Q_p = 0$, $N = 0$ initially and the applied voltage V is increased gradually. The first junction to reach the threshold of $q/(2C_t)$ will tunnel an electron. Assume that $C_1 > C_0 + C_2$ so that the largest voltage drop is on the second junction. Under

these assumptions,

$$V_2(N) = \frac{C_1 V + Nq}{C_t} \tag{2.24}$$

$$V_1(N) = \frac{(C_0 + C_2)V - Nq}{C_t} \tag{2.25}$$

so that at $V = q/(2C_1)$,

$$V_2(0) = q/(2C_t) \tag{2.26}$$

and an electron tunnels out of the island making $N = -1$. In this new state, $V_1(-1) > q/(2C_t)$ so an electron tunnels through the first junction restoring N to 0. For external voltages $V < q/2(C_0 + C_2)$, the first junction remains below the threshold for $N = 0$ and only the above sequence of events ($N = 0 \rightarrow -1 \rightarrow 0$) is possible over the range $q/(2C_1) < V < q/2(C_0 + C_2)$ in the low temperature limit.

The "Coulomb staircase" is the name given to the step structure that appears in the DC I-V curve when the resistance of one of the junctions is much greater than the other. Fig. 2.5 illustrates the step-like increase in the current that occurs each time an N level crosses the threshold for junction 2 at half-integer multiples of the external voltage q/C_1 (assuming $R_1 \gg R_2$ and zero polarization charge) [17].

Transitions occur rapidly—because of the lower tunneling resistance—across junction 2 till $V_2(N)$ is below the threshold $q/(2C_t)$. However, the overall current flowing through the double junction is limited by the slower tunneling rate of junction 1 due to its high resistance so that the current rises slowly after the first step till it reaches the next step. The effect of the capacitance is mainly to change the slope of the step as seen from the figure.

If $R_1 \approx R_2$, the current is only blocked around the origin and increases steadily otherwise as shown in Fig. 2.6. It is clear that, in this case, the ratio of the capacitances does not have a large effect.

When taking the effect of the second voltage source U into consideration, the curve changes dramatically. It is easy to see that if U and Q_p are both present then they represent an effective polarization charge $Q_{eff} = C_0 U + Q_p$. If Q_{eff} is a multiple of q then the curve is unchanged since its effect on V_1 and V_2 can be compensated in N. However, the fractional part of Q_{eff}/q causes a large

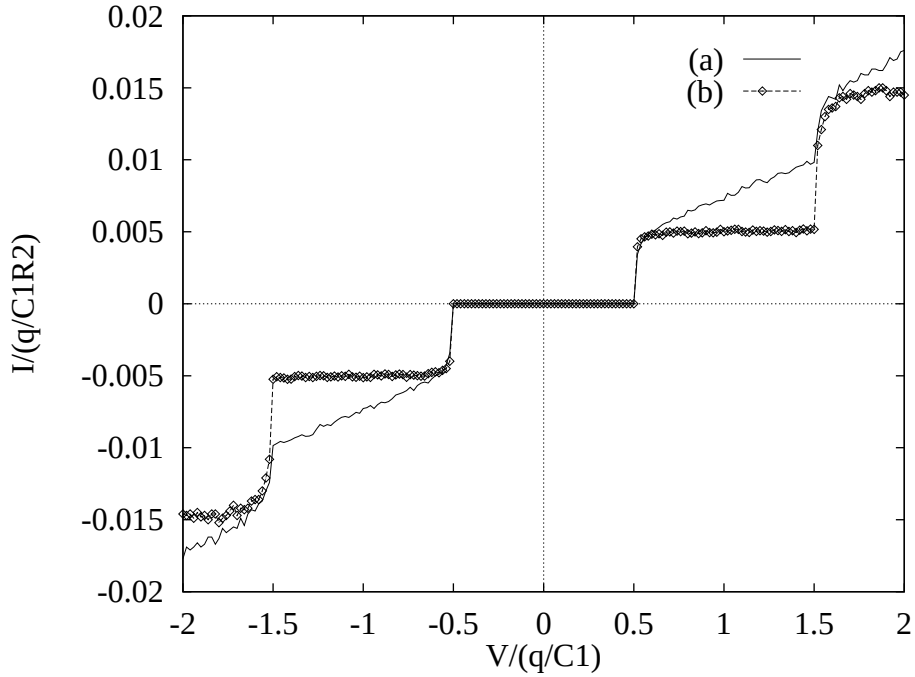

Figure 2.5: Simulation results of the DC I-V curve.
(a) $R_1 = 100R_2$ and $C_1 = C_2$.
(b) $R_1 = 100R_2$ and $C_1 = 100C_2$.

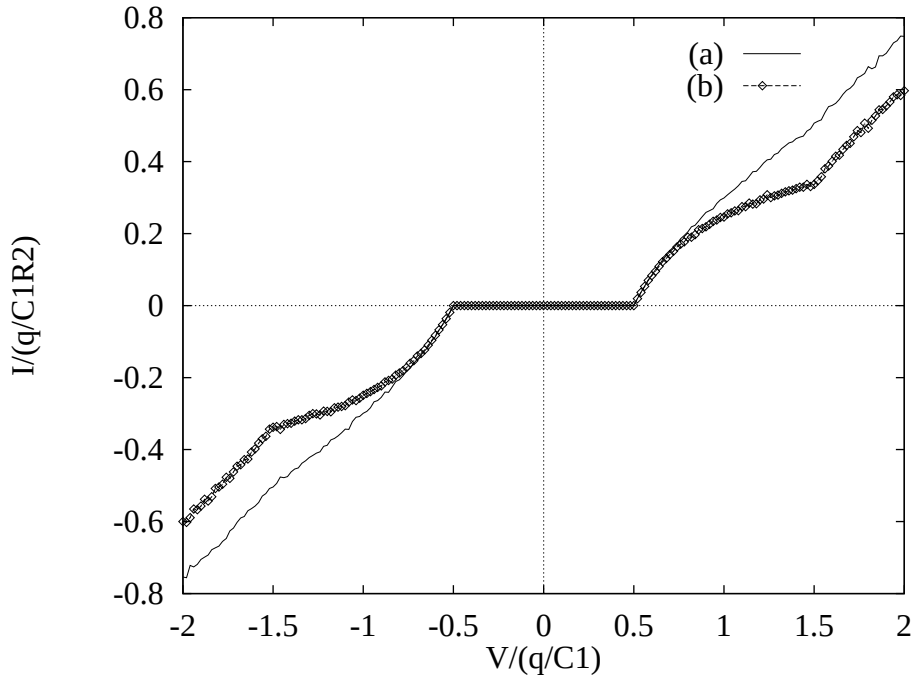

Figure 2.6: Effect of resistances and capacitances on the staircase.
(a) $R_1 = R_2$ and $C_1 = C_2$.
(b) $R_1 = R_2$ and $C_1 = 100C_2$.

difference so that when it equals $1/2$ the current is no more blocked at $V = 0$. This can be easily derived from the formulas of $V_1(N)$ and $V_2(N)$ where it is seen that for $V = 0$ and $Q_{eff} = q/2$,

$$V_1^+(-1) = V_1^-(0) = V_2^+(0) = V_2^-(-1) = 0 \tag{2.27}$$

Any small positive or negative bias across the double junction will thus cause non-vanishing transition rates with no threshold voltage (no blockade region) for the current flow.

A detailed discussion of the staircase curve and the way to estimate the device parameters (C_1, R_1, C_2, R_2) from the experimentally measured characteristics, as well as the effect of the polarization charge and the second source U can be found in Tucker's paper [16]. The main point to stress here is not a detailed quantitative explanation of the curves but a qualitative presentation of the double junction structure.

It is interesting to note that at any bias point ($V = const.$), the effect of C_0U on the current is periodic with period q. When the current conductance, $\partial I/\partial V$, is measured and plotted against U, strong oscillations appear as shown in Fig. 2.7. The existence and reproducability of these oscillations are a good sign of the quality of fabricated structures. Such curves are used experimentally to estimate the value of C_0 from the oscillation period and to investigate the presence of background polarization charge through thermal cycling. Thermal cycling means that after cooling the device to its operating temperature it is returned to room temperature and then cooled and measured again. The amount of background charges and their locations may change due to this process and hence the curves are shifted.

The double junction structure is sometimes named Single Electron Transistor (SET) since it has three terminals as the normal transistor and the 'gate' terminal, U, can alter the DC I-V curve of the 'drain' and 'source'. It is also sometimes named Quantum Dot (Q-Dot) especially when fabricated by a quantum confinement of charge carriers in semiconductors. Although the SET is the most 'famous' device in the field of single electronics, it is not the one that has the most applications. A large number of circuit applications uses not just two tunnel junctions

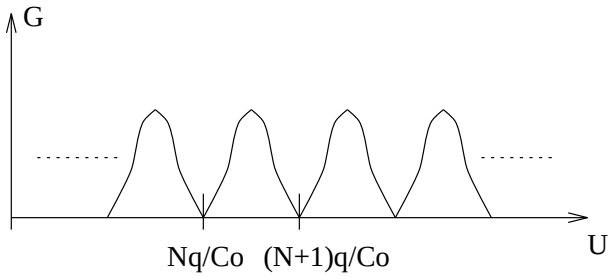

Figure 2.7: Schematic of the Drain-Source conductance oscillations as a function of the gate voltage.

as the SET but an array of junctions or even a two dimensional array as will be seen in the next section. The SET remains however, the basic device in the single electronics domain and maybe the easiest to fabricate.

The presence of several junctions in series reduces an important problem of single electronics known as *co-tunneling*. It means that one electron enters the island of a double junction system through one of the junctions while another electron leaves it through the second junction. This effect may also happen if one electron tunnels through both junctions in one tunneling event [14, 18]. The use of multiple tunnel junctions increases the total tunnel resistance. This enhances the localization of the electron wave function on the island.

2.3 Applications of single electronics

The circuits based on single electronics can be divided into analog and digital applications. Each type of circuits exploits certain characteristics of the devices. It was mentioned in section 2.2.1 that if an SET is current biased, its voltage oscillates at the frequency $f_{SET} = I/q$. The inverse relation is also true. If an RF frequency f is applied to the gate terminal, an electron tunnels from the source into the dot on the positive half cycle and out of it to the drain on the negative half cycle giving the relation $I = qf$. This is what is used for "pumps" and "turnstiles" as discussed in section 2.3.1.

Since the SET is very sensitive to charge variations of the central electrode, this phenomena can be used to make a very accurate electrometer that can sense amounts of charge even less than the electronic charge. The ability of measuring such minute charges allowed others to think about using the SET as a memory

device to store '0' or '1' electronic charge and then to sense it using an electrometer or otherwise. Finally after proving itself in different domains, the SET was thought of as a digital device. The SET can be used to replace the normal transistors in different circuits or, more elegantly, to represent the information bits by single electrons which interact together to give the operation's result. The latter form of logic is now known by the name Single Electron Logic (SEL).

2.3.1 Tunnel junctions arrays, turnstiles and pumps

If a one dimensional array of small tunnel junctions is voltage biased, it exhibits a correlation between tunneling events [19]. In fact, in such an array, when an electron is added to one of the islands the surrounding tunnel junctions capacitances are charged. The charge on the junctions will decay with the distance from the initially charged island and will thus be localized in space over a small number of junctions. Then, if the electron tunnels to another island the whole charge distribution follows it. This distributed charge is usually called a "soliton" since it does not change its shape when it moves as long as it is far from the array edges. Similarly, the lack of one electron on an island and the corresponding distributed positive charge is called "antisoliton". When the array is biased one soliton may enter from the biased edge but the probability of another soliton to enter gets very low because of the soliton-soliton repulsion. However, the repelling force between the biased edge and the soliton drives the soliton deeper into the array and then the next soliton can enter the array. Experimental results justifying the above arguments and showing both time and space correlations in 1D arrays of 15 to 53 junctions were presented by P. Delsing [19]. These experiments allowed also the study of phase locking between the SET-oscillations and an externally applied microwave irradiation. Clear current steps in the DC I-V characteristics corresponding to $I = nqf$, $n = \pm 1, \pm 2, \ldots$ were observed.

Not only phase locking with an external frequency is possible, but the external frequency can also *induce* tunneling into the array. One such system is the turnstile shown in Fig. 2.8. At small V and when U is varied, an electron can only enter the island from the negative end of the bias and leave at the positive end [20]. However, the conduction is not achieved over the whole range of V and U. There

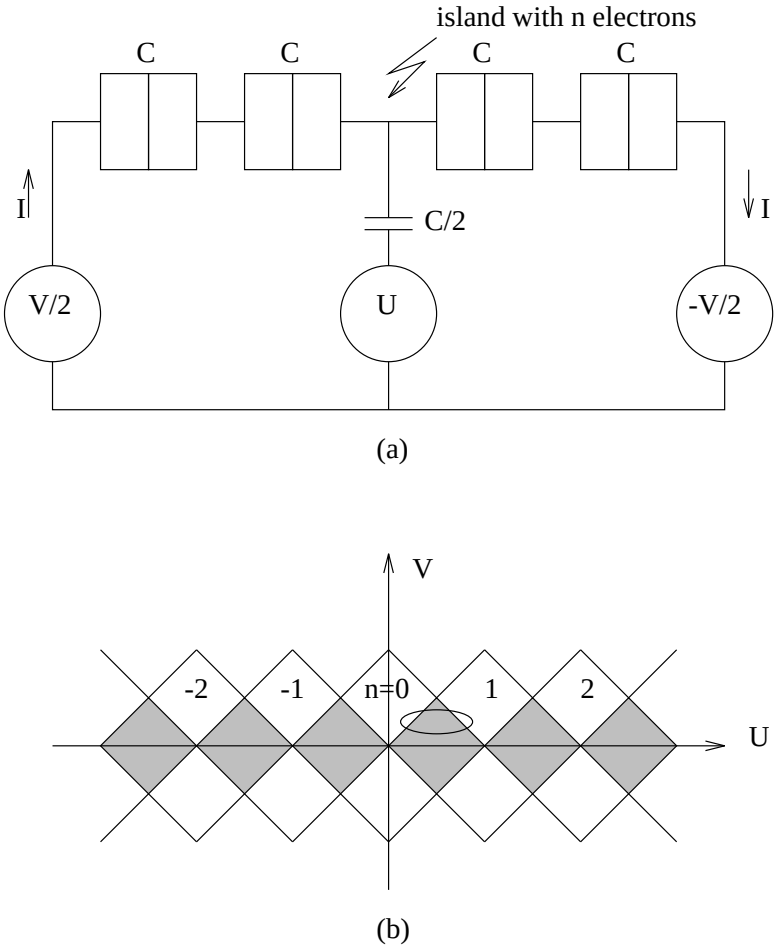

Figure 2.8: The turnstile.
(a) Schematic diagram of a turnstile.
(b) Stability domains in the (U, V) plane.

are some stability domains in the (U, V) plane where the number of electrons in the island is stable and no conduction occurs (a blockade condition). These domains are the diamond shaped areas in Fig. 2.8(b) which overlap together in the hatched areas. Outside these domains, current flows through the device.

Assume that U follows the cycle shown in Fig. 2.8(b) beginning in the $n = 0$ region. As U is increased, it crosses the overlap and enters the $n = 1$ region introducing an electron into the island then when decreased it returns to the $n = 0$ region pushing this electron out to the positive bias terminal. Experiments were performed where an RF signal of frequency f was superimposed with a DC voltage on the gate and a current $I = qf$ was observed [20].

The overlap between every two neighboring domains means that the device contains a hysteresis and thus its operation is irreversible i.e. if one reverses the

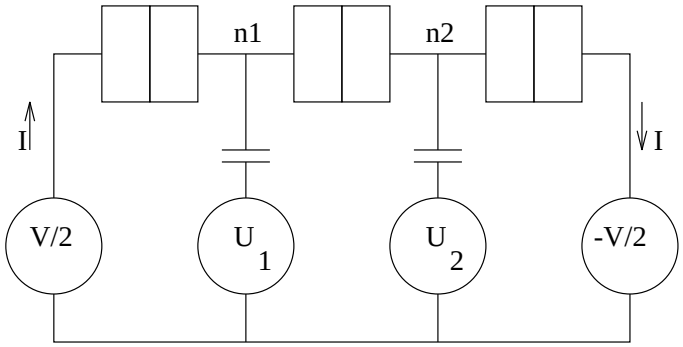

Figure 2.9: Schematic diagram of the pump.

time evolution of U the transfer is not reversed. In fact, this hysteresis allowed some researchers to qualify it as a memory [14]. D. Esteve [20] argued that to have a reversible device more than one control (gate) voltage is needed. The simplest device of this type is the pump shown in Fig. 2.9. It has three junctions biased by the bias voltage V and two gates with control voltages U_1 and U_2. Similar to the turnstile, an RF signal is superimposed on a DC bias on each gate. However, for the pump to operate correctly a phase shift must exist between the signals applied to the two gates. It can be shown [20], that as U_1 and U_2 change slowly ($f \ll 1/(RC)$) with a phase shift $\phi \sim \pi/2$ the system adiabatically follows the energy ground state. If the initial (n_1, n_2) configuration is (0,0), it can be changed to (1,0) then to (0,1) and finally back to (0,0) when the gate voltages accomplish a complete cycle. This process is similar to the one in the turnstile where an electron is pulled from one side and pushed to the other, however the difference is that here it is reversible. If the evolution of U_1, U_2 is reversed (by adding π to the phase shift ϕ) the direction of the current flow is reversed as long as the bias V is low [20].

The importance of reversibility arises from the fact that to have a nearly dissipationless operation reversible devices must be used as discussed by Landauer [21].

The accuracy of both the turnstile and the pump to drive a certain current value was discussed by Esteve [20] and a detailed analysis of the 1D array of tunnel junctions was given by Delsing [19]. It is expected that the accuracy can be $\sim 10^{-10}$ [14] although early experiments gave an accuracy of $\sim 10^{-3}$ [20]. One drawback of these devices that can be easily remedied is the low current values (around $1pA$). Several devices can be connected in parallel to give a total current

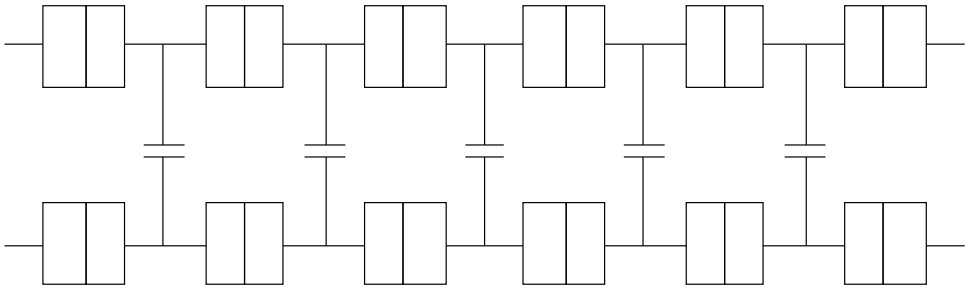

Figure 2.10: Two capacitively coupled arrays forming a current mirror.

in the micro Amperes range. This solution assumes that the fabrication techniques allow easy integration of a large number of tunnel junctions, which is not yet an easy task to fulfill as will be seen when these techniques are discussed. If the integration is however feasible, other interesting ideas can be readily achieved. Fig. 2.10 illustrates two arrays of tunnel junctions where each electrode in one array is capacitively coupled to the corresponding electrode in the other array. When a soliton enters one array the probability that an antisoliton enters the other array increases. So as current flows in one array, the solitons in that array drive antisolitons in the other array giving rise to an equal but opposite current in the second array. This is what is called a Quantum Current Mirror [19]. A Quantum Current Transformer (or current amplifier) can also be achieved by connecting in series one side of a large number of these devices while connecting the other side in parallel. A small *accurate* current can thus be transformed to a larger *usable* value while maintaining its accuracy. The area of such a system is still much less than a similar conventional device.

2.3.2 Electrometer

The influence of the gate voltage on the current of a double junction structure is quite large and can be used to detect small charge variations on the gate coupling capacitor. The electrometer is based on this simple idea. In fact, experiments [20] indicate that the transfer coefficient $dI/d(CU)$ can attain $600pA/q$. The charge noise or charge resolution (different names are used by different research groups) is defined as [14]

$$\delta Q_{min} = \frac{\sqrt{S_I(0)\Delta f}}{\mid dI/dQ \mid} \tag{2.28}$$

where $S_I(0)$ is the low frequency spectral density of the current fluctuations at the electrometer output. The charge noise was measured to be $10^{-4}q/\sqrt{Hz}$ in the above experiments. Its theoretical prediction is about $10^{-5}q/\sqrt{Hz}$, the discrepancy between theory and measurements is attributed to the excess of $1/f$-type noise in the experiments. This, however, is six orders of magnitude better than the corresponding values in the best commercially available semiconductor transistor electrometers. Even the specially designed low-temperature semiconductor devices are 100 times less sensitive than the SET electrometers [22].

A more detailed discussion of the supersensitive electrometry as well as the use of single electron tunneling devices for electromagnetic radiation detection is presented by Averin and Likharev [14, 22].

2.3.3 Memories

Ultra dense memories can be fabricated using single electron devices. Current day dynamic RAMs use charges to store the information on a capacitor. The ultimate density can be achieved if the charge is reduced to just a single electron on a tiny electrode. Moreover, since for single electron devices the electron is trapped on the island in a minimum energy condition, it is stable and such memories could exhibit very long retention time even when the bias is removed. They can be considered as fast EEPROMs.

The analysis of such memories will not be presented here, the interested reader is referred to references [14, 22]. The experimental work is quite impressive already, quoting from a paper's abstract [23]:

> "... with read and write times less than $100's$ of a nanosecond at operating voltages below $2.5V$ have been obtained experimentally. The retention times are measured in days and weeks, and the structures have been operated in excess of 10^9 cycles without degradation in performance."

The "nanomemories" have their own problems however. Room temperature operation is a challenge facing all the single electronics field and specially high density memories. This goal of operating at higher temperature was recently

achieved and a room temperature single-electron memory was announced [24]. Another problem that has been neglected for a long time is the effect of the background charge variations. This problem was addressed recently and a possible solution for ultra-dense hybrid SET/FET dynamic RAM was presented [25]. An RS flip flop which is fairly independent of offset charges and returns the correct bit 97% of the time was also presented by Hadley *et al.* [26].

2.3.4 Digital applications

Single Electron Transistor logic

Digital applications of single electronics include the use of SETs as replacement for the normal transistors in what is known as Single Electron Transistor logic (SET logic). In order to have a three terminal device a gate is coupled to the central island via a capacitor or a resistance [27]. The SET operates mainly as a switch and the fact that SETs may exhibit negative transconductance allows the implementation of complementary circuits using transistors of a single type [27, 16]; there is no N and P-type in metallic SETs. However, direct reproduction of CMOS gates is impossible because SETs cannot be open in as wide a range of gate voltage as the FETs [28]. A discussion of the ultimate performance of the SET and the limits imposed on its operation and geometry is given by Lutwyche and Wada [29]. They conclude by proposing an ideal geometry for SETs and giving a possible planar fabrication process for its realization. A more detailed analysis of specific circuits is presented by Korotkov *et al.* [30]. In another paper [28], the same group presents a complete set of complementary logic circuits and estimates its maximum operation temperature, switching speed, power consumption, noise tolerances and error rates. They also show how to calculate the parameters margins of the basic gates.

Tucker [16] proposes a double-gate SET. One of the gates is either connected to the supply voltage or to the ground so that the switch is an "N switch" or a "P switch" respectively. The other gate represents the input and the drain voltage is the output. He presented a complete logic family and discussed a possible fabrication technique and the problem of background charge variation.

Single Electron Logic

The other form of digital applications is the Single Electron Logic (SEL). Information bits are coded by the presence or absence of extra single electrons in the islands. Averin and Likharev presented one family of SEL [14]. Nakazato and Ahmed recently proposed another family which they called single-charge injection logic and gave also a third approach: single-electron Binary Decision Diagram (BDD). Their experimental results show clear switching characteristics [11]. Ancona [31] focused on locally interconnected synchronous networks and proposed several single-electron digital circuits. Although SEL may give the lowest possible energy consumption [22] and a very high packing density, potential problems exist [16]:

1. If thermal fluctuations cause one unwanted tunneling event the expected result is completely destroyed. This limits the operating temperature to low values, $k_B T < 0.01 q^2/2C$, which means that even with a total capacitance as low as $1aF$, temperature may be limited to the range below $10K$ for reliable operation.

2. The single electron existing at the output node of one gate must induce enough voltage to charge the input capacitances of subsequent stages. Fan out may be very limited.

The fan out problem together with the interconnection problem which may be present in such a very highly packed system lead to the ideas of wireless logic given in the next section.

2.4 Problems and proposed architectures

In addition to the traditional way of thinking about replacing the FET transistors in todays circuits with SETs or the use of SEL, the single electronics field has its own architectures due to its particular characteristics and the problems that it is encountering. The main problems facing SET discussed here are interconnections, fabrication difficulties and background charge variation.

2.4.1 Interconnection problems

The interconnection problems arise naturally from the large number of devices expected to be on the chip. With current CMOS technologies having several millions of transistors per chip, wiring is a problem. Technologies use several metalization layers and reliability drops while layout and fabrication complexity increases rapidly. What would be the case if we have three or four orders of magnitude more devices per chip?

More interconnections means also more capacitive loads to charge and more heat to dissipate which may lead to limitations on the speed of operation. A detailed analysis of such effects is presented by Meindl [32].

One possible solution to interconnection problems is to have a sort of wireless interaction between the devices. Proposals for Coulomb force interaction [33, 34, 35, 36], electron spin interaction [37, 38], electron-photon interaction [39, 40] and Q-dots interacting with an external electric field [41] are presented and each one has its own merits and disadvantages as will be discussed later. These proposals alleviate the interconnections problems and —using the communications terminology— allow a much larger "bandwidth" to be used, since the possibility to pack a large number of devices in a small area and to transfer the information in parallel can be viewed as a bandwidth increase. However as explained by Bandyopadhyay and Roychowdhury [38], there is a power limitation problem now since these schemes are edge-driven (the power is only entered at the edges of the circuit with no supply in the center). So the problem of interconnection limitation is solved on the expense of power limitation.

2.4.2 Fabrication problems

Fabrication problems can be divided into two classes:

1. Whether it is possible or not to fabricate the device given the current technology?

2. How *accurate* the fabrication process is?

The possibility to fabricate smaller devices is improving and new techniques are developed every day [42, 43, 44, 45]. However the variation in the fabrication

parameters is a fact that engineers have to live with and provide adequate noise margins to compensate for it. This means that normally one can view the device or the circuit as having the nominal parameters with some noise added to it. Using the communications terminology again, it is assumed here that this noise can be modeled as Additive White Gaussian Noise (AWGN). The term AWGN means that the probability density function of the noise amplitude is assumed to be Gaussian with zero mean and that the power spectral density of this noise is constant over all the frequency range.

2.4.3 Background charge problem

As for the background charge problem, only few attempts tried to circumvent it [25, 26]. Otherwise, designers chose just to ignore it. This charge can be viewed as having an influence on each device by a uniform probability distribution within the interval $[-q/2, +q/2]$ [13]. Viewed at the circuit level (composed of a large number of devices) one gets a large number of *independent* uniform probability distributions influences. (Independence of the probability functions is due to the randomness and the independence of the impurities positions). The collective effect of this large number of variations is equivalent to a Gaussian zero-mean noise as stated by the *central limit theorem* [46].

The discussion above suggests that the wireless SET logic can be viewed as a power-limited system with AWGN and that all the theory available in the communications field is applicable to this noisy system to achieve a good performance.

2.4.4 Communication theory applied to Single Electronics

Several modulation schemes are studied in the communication textbooks and it is noted that M-ary orthogonal signals are the best suited for power-limited systems [47]. Here 'M' indicates the number of different symbols (for binary M=2) and two signals are said to be orthogonal if their cross-correlation is zero. As M increases a smaller signal power and hence a smaller Signal to Noise Ratio (SNR) can be used up to the limit of $ln2$ while maintaining the same probability of error in the signal detection. This is the limit predicted by the communication theory before the introduction of reversible and nearly dissipationless computation

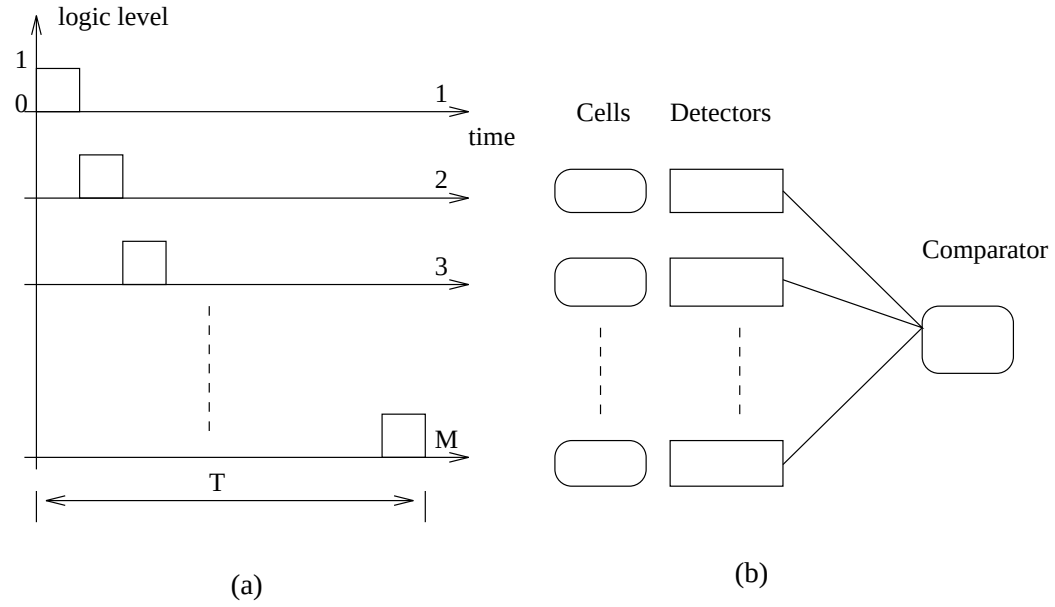

Figure 2.11: PPM signals and their detectors.
(a) PPM signals (T is the symbol period).
(b) Detectors forming a *matched filter*.

and communication discussed by Landauer [21] suggesting that much lower limits can be used. What is considered here however, is the normal dissipative logic. Therefore, the $ln2$ limit is valid and for a certain required error probability, as M increases the SNR needed decreases at the expense of the ratio of bit rate to bandwidth.

A possible suggestion is the use of orthogonal PPM (Pulse Position Modulation) signals as shown in Fig. 2.11(a). These can be easily mapped to the SET world just by having a number of Q-dot cells equal to the number of positions needed and encoding the presence of the pulse in a certain position by a logic '1' in the corresponding cell. This can be mapped to any of the wireless proposals mentioned above. The communication theory with all its benefits can be applied to the single electronics logic as long as the system remains *linear* in the sense of system engineering. This means that the superposition property must hold true which translates to the following simple relation: if $f(x)$ is the output due to x and a and b are constants then we must have $f(ax + by) = af(x) + bf(y)$.

The proposed system is quite simple. The probability of error can be arbitrarily small by choosing a large M. The optimum detectors that can make the maximum-likelihood decision and give the correct answer are just a number of

Scanning Tunneling Microscope (STM) tips or electrometers or photodetectors (depending on the cells used), one for each cell. They detect the logic value in the dots and the one with the highest output is the correct one. Even if noise causes some value to exist in the wrong dots, this "matched filter" design will probably give the correct answer. A schematic of this idea is presented in Fig. 2.11(b). If the noise is however quite high and the power is really limited as discussed by Bandyopadhyay and Roychowdhury [38], one can use the idea of *regenerative repeaters* where, after the signals begin to deteriorate in the logic path, a detector (repeater) is put to restore the power level. These repeaters will be the only parts of the circuit requiring external wiring besides the primary inputs and outputs. In order to further understand this idea more details about the different wireless proposals are presented in the next section.

2.4.5 Previously proposed wireless systems

Bistable nanowires and cellular automata

Lent, Tougaw, Porod and Bernstein [33, 34, 35, 36] proposed a simple scheme for implementing wireless logic. The basic cell is shown in Fig. 2.12(a). It is composed of five quantum dots with two extra free electrons (shown as dark spots) which can tunnel between the dots. The minimum energy configuration is achieved when the two electrons occupy opposite corner dots because of their mutual repulsion. This polarization of the cell may be used to encode logic one or zero as shown in Fig. 2.12(b). If two such cells are put close together the mutual repulsion between electrons in the first cell and those of the second cell causes the two cells to have the same polarization. Fig. 2.12(c) shows an array of cells where the first cell is considered to be the input. If this input cell changes its polarization under the influence of an external input the polarization of the next cell changes and this change propagates along this "binary wire". This phenomena of nearest neighbor interaction can be readily used in cellular automata [34]. Multiple neighbor interaction can be used to implement multi-input logic gates like the majority gate which can be programmed to give an AND/OR gate [35]. The problem of wire crossing was addressed and solved enabling larger circuits like full adders to be designed [36].

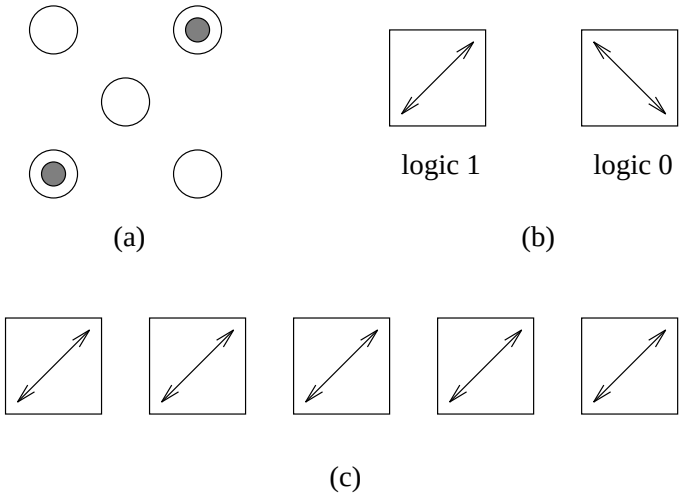

Figure 2.12: Bistable cells and nanowires.
(a) The basic cell with two extra electrons.
(b) The possible two polarization states.
(c) A linear array of cells forming a binary wire.

Despite the elegance of this proposal it lacks a very important feature for logic devices: I/O isolation. The interaction between two cells is bidirectional, the input cell influences the output cell in the same manner as the output influences the input. In a long binary wire, when a signal is applied so that the input cell changes its polarization the second cell is in a meta-stable state between its right neighbor with one polarization and its left neighbor with the other polarization and thus it may not flip to the correct binary state [38]. This situation is even worse in the fan-out of one signal into two channels proposed by Lent *et al.* [34] where the cell is coupled more effectively to its successors than to its predecessor as discussed by Landauer [48]. Other questions concerning the practicality of such devices are also posed by Landauer: "How do we place exactly two electrons on each *cell*? How is that number controlled and/or restored later on, in the presence of leakage, α particles and cosmic rays? Where is the compensating image charge? Is it worthwhile replacing the ordinary wires in computers by long arrays of interacting dots, with their greater sensitivity to defects?"

Spin interaction

Bandyopadhyay and Roychowdhury [37, 38] discussed the possibility to use the electron spin to encode binary information. Single electrons in arrays of quantum dots can have a spin-spin interaction so that an electron having a spin up in one

dot forces the electron in the next dot to have a spin down and binary information can be transferred. This proposal and the one presented above are quite similar and have a lot of common problems. However, this one can solve the meta-stable state of a middle cell in a multi-neighbor interaction situation (for NAND and NOR gates), where the cell faces different polarizations from its right and left neighbors, by introducing a small magnetic bias in one direction (this bias is in fact needed to define the two spin states [38]).

The two proposals have yet another problem in common which is the "unbalanced logic gates" studied by Lusth *et al.* [49]. Both schemes compute by relaxing to the energy ground state of the whole system. However, certain input combinations give rise to higher energy ground states than others. This unbalance can lead to erroneous operation as explained by the examples given in the reference.

Electron-photon logic

Nomoto *et al.* [39, 40] proposed a novel logic device with electron-photon interaction in two coupled quantum dots. The device can perform (N)AND and (N)OR operations simultaneously. The I/O is accomplished by the irradiation/absorption of photons. The operations are performed by the relaxation of the electrons to the ground state. The error probability per device was estimated to be 0.2 at a temperature of $77K$ and so a proposition was presented to use an array of device units in order to reduce the overall error probability. The device needs a separate reset after each operation which may slow the system performance as discussed before. The fabrication issue was discussed but it remains an open area of further investigation.

Wireless SEL biased by electric field

Korotkov [41] proposed the system shown in Fig. 2.13. A chain of closely located conducting islands serves as the basic element of the device. In the presence of an externally applied electric field, if an electron-hole pair is generated in the middle of the chain the electron is dragged to the end of the chain in one direction and the hole in the other direction. This chain polarization is considered to represent logic '1' while logic '0' is represented by an unpolarized chain. Signal propagation

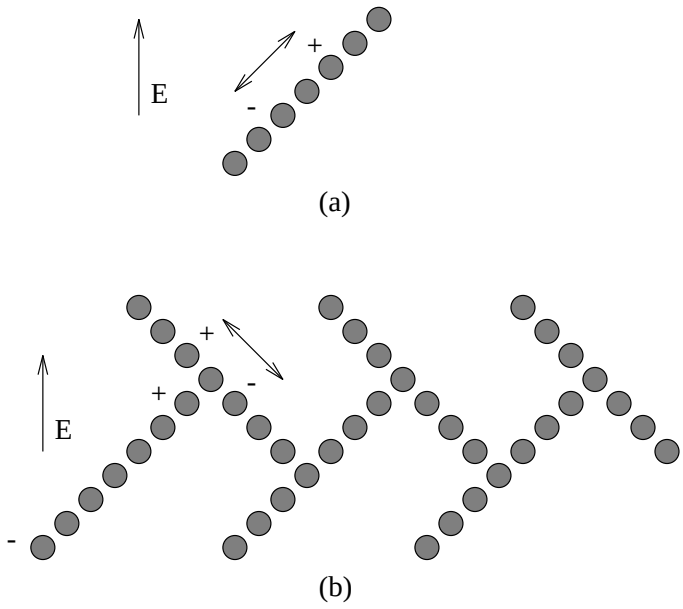

Figure 2.13: Wireless SEL biased by an electric field.
(a) Basic chain of conducting islands.
(b) A line of chains propagating the signal form left to right.

can be achieved by cascading several chains as shown in Fig. 2.13(b). Provision of the OR and AND function was presented but the implementation of the inversion was not straight forward. It was possible to produce the function $\overline{A}$ AND B *if* the signal from input A arrives at the interaction point before the signal from input B (which can be set to 1 to get $\overline{A}$ at the output). This temporal dependence is clearly not feasible to use in large circuits where the propagation delays along different logic paths are not controllable.

Atom/molecule switching

The ultimate miniaturization of devices is to use a single atom as the switching device. Wada *et al.* [50] simulated the behavior of such an atom relay. The principle of operation is that a switching atom is displaced from an atom wire under the influence of the electric field induced from a switching gate as shown in Fig. 2.14. The introduced gap cuts the electron propagation along the wire. NAND, NOR and memory cells were proposed. This logic family is estimated to have an operation speed in the terahertz range. A fairly complete comparison of MOSFETs, quantum devices, SETs, molecular devices and the atom relay was also presented and the main conclusion is that the atom relay gives the ultimate

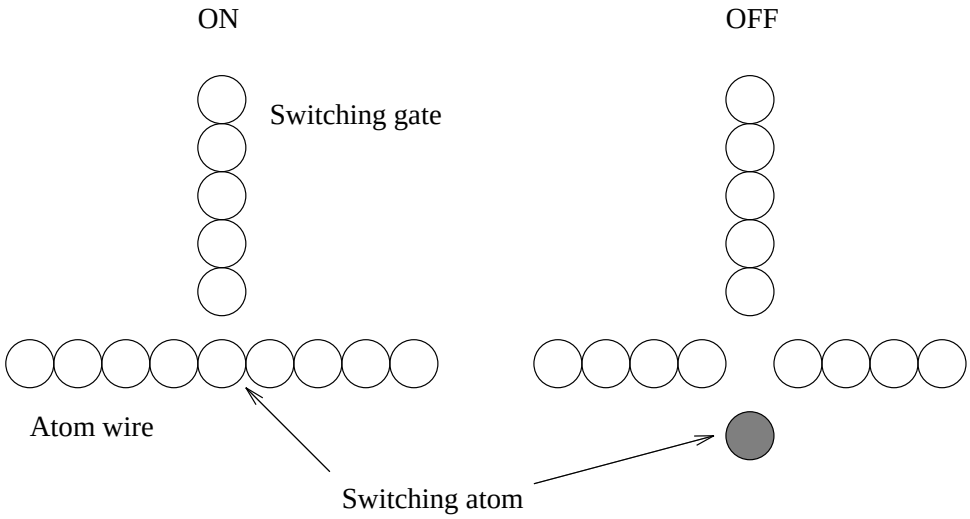

Figure 2.14: Schematic of the atom relay.

packing density and speed of operation but the fabrication technology has not yet reached the stage where such devices can become a reality. The SETs emerge from this comparison as the second best choice.

Discussion in view of the ideal logic characteristics

It was noted out before [38, 41, 48] that the wireless proposals may lack the unidirectionality property required in any logic family. A solution for this is to continuously increase the spacing between the cells in order to have a higher coupling to the left neighbor (the input) than to the right neighbor (the output). This solution is applicable to the systems of Lent [33] and Bandyopadhyay [38]. The systems of Korotkov [41] and Nomoto [39] are inherently unidirectional. This does not mean however that these two latter systems have no problems. The system proposed by Korotkov [41] may not function as described since it is not clear how the electron-hole pair will be generated in the chain. The external field cannot give enough energy to the dots to cause an electron-hole generation since it will be basically applied across the barriers between the dots [51]. Another energy source is required. The first guess would be the use of light to energize the electrons but in practice it would be hard to achieve a large number of light beams focused on certain dots in the system where generation should occur. Even if it is feasible this would mean that one would know *a priori* the locations where a polarization is to occur, i.e. one should know the results of the logic circuit by

some other means and hence, there is no need for this circuit.

Another real problem for this system is its very high sensitivity to the variation of fabrication parameters. As indicated, a variation of the dot radius by 5% causes the logic output to be an AND instead of an OR function [41]. Unless these problems are solved somehow this system cannot be practically realized. As for the system of Nomoto [39], it shares with that of Korotkov [41] the problem of how to focus a large number of light beams on several narrow areas (few nanometers square each).

For the first two systems the continuous increase of spacing between the cells cannot be carried on indefinitely since it decreases the interaction between them and may stop the signal propagation. This reduces the number of cascaded cells allowed in the logic family. Also a note was made [38] about the power requirement and how it may limit the number of cells. Both of these points will lead naturally to the idea of regenerative repeaters discussed earlier. However, the calculations presented by Bandyopadhyay and Roychowdhury [38] for the number of cells in one logic block were based on the formula giving the amount of energy required per input port as $(B/N)k_BT\ln 2$ (B = total number of cells in a block, N = number of input ports and $k_BT\ln 2$ = energy dissipated per cell).

This is not quite correct since not all the cells would be switching together with every input. One would have rather a much smaller portion switching. This is called the *circuit activity* and is usually used to calculate the power consumption in CMOS circuits. Depending on the logic design this number can vary between say 5% and 30%.

Let us take the same numbers as Bandyopadhyay [38], $N = 10$ with the maximum energy to be applied to one cell in the order of q^2/C with $C = 10^{-19}F$ and apply them in the more exact formula, $B = (Nq^2)/(aCk_BT\ln 2)$ (where a is the percentage of activity), if we let $a = 0.10$ we get $B \approx 8900$ at room temperature. After this number, repeaters must be added. Note however that the logic depth must not be very high in one logic block since that would lead to the decrease of the interaction force with each logic level. The logic blocks should rather be used to provide a maximum amount of parallelism which has the additional benefit of increasing the speed of operation.

2.5 Conclusion

Single electronics is a growing field of study that may prove itself to be the sole replacement for CMOS technology. Several problems still exist and are open for research. Fabrication techniques present a challenge and will be addressed in details in the next chapter. Till recently no simulation tools were available for single electron devices and even now the available tools [17, 52, 53] are not quite developed to handle large circuits of more than tens of tunnel junctions. If the single electronics is to present the highest possible packing density, tools must exist to support the designers in doing so. New ideas for applications either in digital or analog circuits are also needed in order to guide the fabrication groups and as discussed before interconnections and power dissipation are among the important issues to handle at the present time.

Chapter 3

Nanofabrication

3.1 Fabrication techniques

Methods used for fabrication of single electron devices can be classified into two main categories: the all-metal devices and the semiconductor devices. A brief description of each of these classifications is given below.

3.1.1 Metallic devices

This is the easiest approach. The different electrodes and islands are made of a metal and tunnel barriers are usually made from the oxide of the same metal. Obviously, the junction capacitances depend on the electrodes' areas. The early experimental work used capacitances in the order of femto-Farads and hence cooling to the milliKelvin temperatures in dilution refrigerators was necessary [12]. It was also necessary at these temperatures to apply a magnetic field in order to prevent the metal from switching to a superconducting state. Smaller device sizes can now be achieved by using e-beam lithography.

E-beam can achieve high resolutions and experiments to deposit lines with $30nm$ width and $50nm$ spacing were reported by Lee and Hatzakis as early as 1989 [54]. An all-chromium single electron transistor fabricated using e-beam lithography and shadow evaporation technique was recently reported [55]. Even smaller sizes —atomic and nanometer scale— are possible using proximal probes: probes of Atomic Force Microscopy (AFM) and Scanning Tunneling Microscopy (STM). One can achieve local modifications with nanometer or atomic spatial

resolution by controlling the perturbations induced by the proximal probe tip on the sample [56, 57].

Matsumoto *et al.* [44, 45] used an STM/AFM nano-oxidation process for the TiO_x/Ti system to produce single electron transistors. This nano-oxidation is achieved by applying a negative bias to the tip with respect to a thin Titanium film on an insulating substrate. The resultant electric field dissociates the water molecules that adhered to the surface of the metal from the air. The oxygen attacks the metal to oxidize it while hydrogen is liberated. The extremely small tunnel junctions which are possible to fabricate by this technique allowed the Titanium based SET to operate at room temperature.

The method used by Matsumoto *et al.* is not however very well controllable. This is clear from their reported results for the TiO_x/Ti barrier height and dielectric constant of TiO_x. In one paper [44] these numbers were reported as $0.308eV$ and 5 respectively while in the other paper [45] they were $0.285eV$ and 24. This variation may be due to the choice of the metal (Titanium) which does not form one type of oxide but a number of oxides (TiO_x).

Snow and Campbell [58] presented a much better approach which does not depend on the formed oxide. It is based on the fact that the chemical composition is not important but the important thing is the electrical behavior of the device. So, while oxidizing, in-situ measurement of the electrical properties are performed and once the required properties are achieved the oxidation is stopped. The materials in which selective oxidation is possible are: Titanium, Niobium, Chromium, Aluminum, Silicon and Gallium Arsenide [44].

3.1.2 Semiconductor devices

Fabrication of single electron devices using semiconductors was done through two different paths. The first one was the use of Hetero-junction devices where a two dimensional electron gas (2DEG) is formed and then using split-gates the electrons are depleted from some regions and the remaining constriction forms the Q-dot. The second path is the use of silicon as base material.

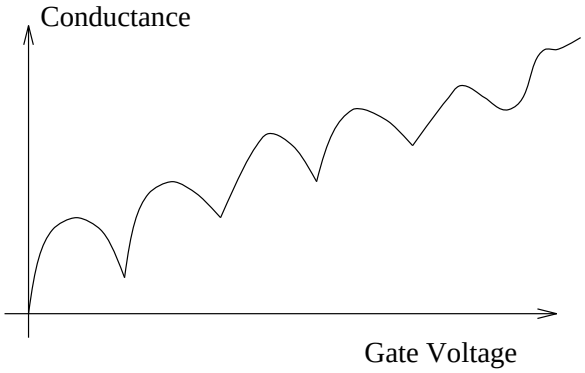

Figure 3.1: Conductance oscillation for a semiconductor device.

Constriction in 2DEG

Early experimental work in this area was presented by van Houten *et al.* [59] and Kouwenhoven [60]. A unique feature of 2DEG is that it can be given any shape using lithographic techniques. A pattern can be etched away and a permanent removal of the electron gas results. Alternatively, a reversible electrostatic depletion can be induced by a patterned gate electrode.

These systems differ from the metallic junctions in a fundamental way. In metallic islands the electron energy level separation is much smaller than the thermal energy and hence the energy spectrum may be treated as a continuum. In semiconductors this is not true. Because of the lateral confinement, the conduction band is split into a series of one-dimensional sub-bands [59]. To introduce a new electron it is necessary to circumvent the Coulomb blockade energy and the quantum separation energy. Resonant tunneling may occur due to this energy separation.

Furthermore, as the gate voltage is swept the barrier heights of tunnel junctions change. This change is evident because it is this same gate voltage that originally confines the dot so when it is swept a different degree of confinement is reached. The drain-source current is affected by this and the conductance oscillation are not simple periodic oscillation as those for the metallic junctions but normally rise as shown in Fig. 3.1 and are gradually smeared.

One major disadvantage of field-induced confinement is that it cannot create quantum dots small enough to permit high operating temperatures [61].

Silicon SET

Silicon is the main stream material used in micro-electronics and its use for SET fabrication was investigated by different research groups [42, 43, 62, 63, 61]. Similar to metallic junctions, small sizes can be achieved by e-beam lithography or proximal probe manipulation. The kinetics of oxide formation using AFM/STM probes were studied [64, 65, 66]. It is important to note however that the barrier height between silicon and silicon dioxide is quite high and therefore the tunnel junction cannot be made totally of SiO_2 or the tunneling current will be very low. Actually it is enough to oxidize a silicon nano-wire from the side and to leave a small Si constriction which is depleted from carriers (due to its very small size) and hence represents the tunnel junction.

This idea of sideway oxidation of a silicon nano-wire was used by Takahashi *et al.* [42, 43] who defined a short ($\approx 50 \rightarrow 200nm$ in length) $20nm$ wide silicon wire using the technique of e-beam lithography with image reversal by Electron-Cyclotron-Resonance (ECR) plasma reported by Kurihara *et al.* [67]. The lateral oxidation of the Si wire stops when the mechanical stress of the growing SiO_2 (which has a larger volume than Si) is balanced by the stress from the Si remaining in the middle region and further oxide formation is suppressed. After constricting the wire by lateral oxidation, a poly-Si top gate is formed. The relation between the designed wire length and gate capacitance is claimed to be linear but the reported measurements are not very convincing and show a large deviation from the claimed behavior. The capacitance remained however small enough to allow room temperature operation. It is clear that this approach of stress dependent oxidation is not very well controllable and hence large deviations in the device parameters may result.

In order to have a more controllable process, Leobandung *et al.* [62, 63, 61] developed a new method to fabricate quantum dots on SIMOX (Separation by IMplanted OXygen) wafers by using e-beam lithography and reactive ion etching. The resulting dots are larger in size and operate at lower temperatures. The same group introduced also a single hole quantum dot [63] which can be used in complementary circuits with their single electron equivalent.

In these silicon Q-dots, single electron charging energy and quantum energy are

comparable and if the size becomes smaller (to raise the operation temperature) quantum effects will be the dominant factor responsible for the discrete energy levels [62]. Coulomb energy will become irrelevant then. This fact is considered as "bad news" for designers since the quantum energy is inversely proportional to the square of the dot size and hence any small variation in the size due to fabrication tolerance will result in a large deviation in the device parameter. That is why some researchers do think that silicon (and semiconductors in general) may not be the best choice to implement SETs for real circuit applications. Semiconductor SETs however present a very interesting problem for device physists to study.

3.2 Estimation of electric parameters

Several aspects of the fabrication influence the electric parameters of tunnel junctions. The choice of the materials and their geometric layout are of extreme importance in the determination of the capacitance and tunnel resistance values. This is due to the fact that the capacitance depends on the dielectric constant and the geometric shape of the insulator and the resistance depends in addition to that on the barrier height and the potential difference across the junction. The equations giving the relations of the tunnel resistance and capacitance for a certain junction are presented here. Then, some numerical examples are given to conclude the discussion.

3.2.1 Tunnel resistance equations

The study of tunneling is as old as the quantum theory itself. Tunnel diodes were introduced in the late 50's [68]. In the 1960's, a lot of experiments were done. Giaever [69] presented a detailed explanation of the experiment preparation and the measurement procedures while Duke [70] gave the basic theory of metal-barrier-metal tunneling. Based on this work, Simmons [71, 72, 73] derived several equations giving the tunneling conductance for different values of the voltage applied across the junction whether the junction is formed by similar or dissimilar electrodes. Our discussion here will be limited however to the case of similar electrodes. The main advantage of these equations is that they accurately

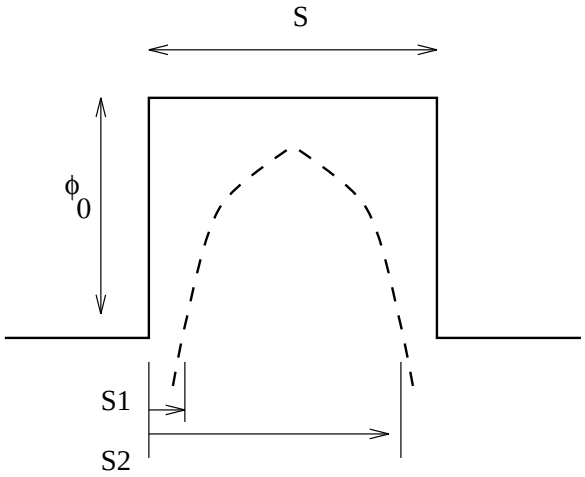

Figure 3.2: Schematic of a rectangular barrier (solid) and the effect of the image force (dashed).

describe the effect of what is known as the "image force" on the tunneling current.

The image force is due to the fact that when an electron exists between two parallel and closely spaced electrodes, it polarizes both of them. The polarization charge, as a result, influences the potential of the electron within the electrode separation. The effect of this "image" potential is to reduce the height and width of the potential barrier between the electrodes and to round off its corners. Fig. 3.2 illustrates this effect as well as the different parameters involved in its determination. These parameters are defined as:

s	Thickness of the insulator
s_1, s_2	Limits of barrier at Fermi level
Δs	$s_2 - s_1$
ϕ_0	Height of rectangular barrier
ϕ	Mean barrier height
ϵ_r	Dielectric constant
A	Area of the junction

According to Simmons, when the barrier height is expressed in electron volts and the distances in Angstrom, the relation between the current density J and the voltage across the tunnel junction V is

$$\begin{aligned} J &= \frac{6.2 \times 10^{10}}{(\Delta s)^2}(\phi \exp(-1.025 \Delta s \phi^{1/2}) \\ &\quad - (\phi + V)\exp(-1.025 \Delta s (\phi + V)^{1/2})) \end{aligned} \tag{3.1}$$

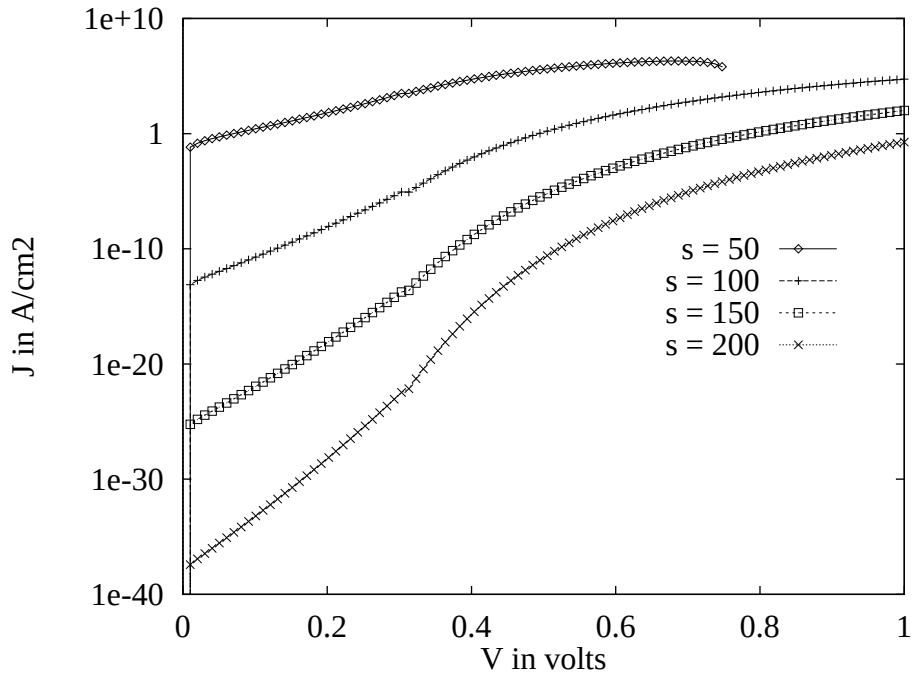

Figure 3.3: J-V curves of a tunnel junction when insulator thickness is varied.

This is a nonlinear relation between J and V as shown in Fig. 3.3.

At low voltages (much less than ϕ_0), the tunnel resistance is nearly ohmic and the equation can be reduced to [71]

$$J = \frac{3.6 \times 10^{10}}{\Delta s}\phi^{1/2} V \exp(-1.025\Delta s\phi^{1/2}) \tag{3.2}$$

where

$$\phi = \phi_0 - \frac{5.75}{\epsilon_r(s_2 - s_1)} \ln(\frac{s_2(s - s_1)}{s_1(s - s_2)}) \tag{3.3}$$

and

$$s_1 = \frac{6}{\epsilon_r \phi_0} \tag{3.4}$$

$$s_2 = s - \frac{6}{\epsilon_r \phi_0} \tag{3.5}$$

It is this ohmic conductance, JA/V, that can be used in the equations giving the rate of electrons tunneling according to the 'orthodox' theory (sections 2.2.1 and 2.2.2). As for the capacitance of the junction it can be directly estimated

assuming a parallel plate capacitor as

$$C = \epsilon_r \epsilon_0 A/s \tag{3.6}$$

These theoretical estimates can be used to guide the fabrication process. In fact, a recent study [74] made a comparison between experimental and theoretical results for SETs and they appeared to be in good agreement.

3.2.2 Numerical examples and discussion

Small capacitances (in the order of atto-Farad) are needed for single electron devices to operate properly at high temperatures. For the case of a parallel plate capacitor as shown in Fig. 3.4(a,b), only three parameters are possible to vary: ϵ_r, A and s. To achieve a small capacitance we can reduce ϵ_r or A or increase s. However, ϵ_r and s are present in the exponential term of the tunnel conductance. As any of these parameters is increased the conductance decreases rapidly. This would lead to extremely low tunnel currents and switching speed in the devices. Thus it is not advisable to increase s but ϵ_r can be decreased leading to smaller capacitances and higher tunneling conductances. The choices for ϵ_r are however limited since changing ϵ_r means changing the insulating material used. Other considerations (chemical, technological, economical, ...) may thus prohibit such a choice. The remaining parameter, A, is a better controlling parameter to use since it decreases both the capacitance and the conductance in a *linear* manner. The decrease in the conductance can be compensated by changing the barrier height. Although this means changing the materials used too but it is easier to accomplish. It does not depend only on the insulator but also on the electrodes so its value can be, more or less, engineered easily.

Fig. 3.4 illustrates different possibilities to decrease the capacitance by decreasing the area. It is clear that the use of layers stacked on top of each other (Fig. 3.4(a)) cannot achieve very small areas. It requires a highly sophisticated lithography technique and even if the small area is achieved the alignment of the layers may cause a problem. The side capacitor shown in (b) can achieve much smaller capacitances since it depends on the thickness of the layer deposited on the

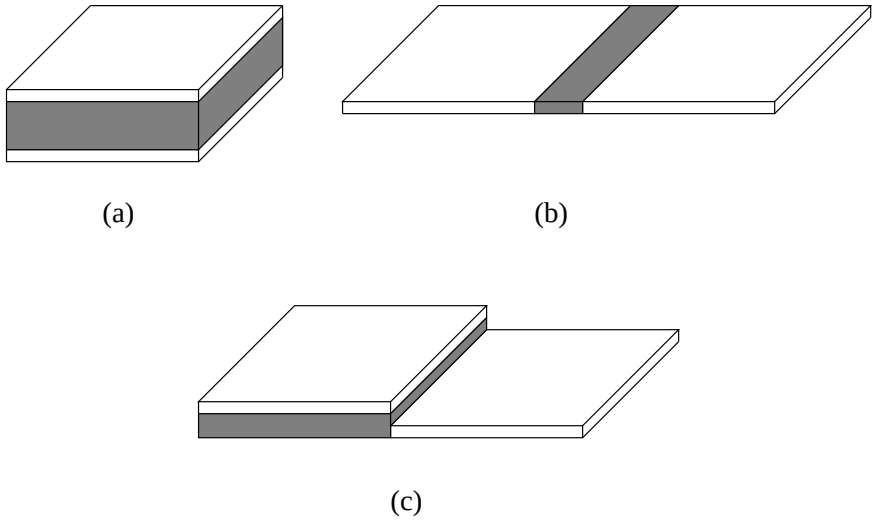

Figure 3.4: Different possibilities to achieve small capacitances.
(a) Normal parallel plate capacitor.
(b) Side capacitor.
(c) Step edge cut off capacitor.

Table 3.1: Values for the junction parameters.

Parameter	Value
C	$0.44aF$
s_1	3.89Å
s_2	196.10Å
Δs	192.2Å
ϕ	$0.261eV$
J/V	$1.6 \times 10^{-36} A/Vcm^2$

substrate (which is a fairly well controlled technology parameter). The Step Edge Cut Off (SECO) capacitor is a variation of the side capacitor recently introduced by a German group [75, 76]. Capacitances as low as $1.5aF$ are achieved using the SECO process with a lithography giving a $75nm$ line width. A three dimensional calculation is needed to estimate the resulting capacitance in a SECO process. That is why the calculations presented here are limited to the side capacitor configuration.

For a Ti/TiO_x interface with interface height= $10nm$ = 100Å, $s = 20nm$ = 200Å and interface length equal to s ($\phi_0 = 0.308eV$ and $\epsilon_r = 5$ [74]), the results are as shown in Table 3.1.

Keeping the interface length equal to s makes the capacitance dependent on ϵ_r and the interface height only. It is clear from these calculations that the conductance value is quite low while the capacitance value is suitable for room tem-

perature operation. The conductance value can be increased without affecting the capacitance if the insulator thickness s and the interface length are decreased together keeping them equal. Assuming the new value to be $s = 10nm = 100\text{Å}$ then $J/V = 4.12 \times 10^{-12}$. This example shows that the capacitance and conductance values can be engineered to a fairly good degree. It would be interesting if a complete study taking into account the chemical, technological, economical, ... aspects and involving the variation of the materials and dimensions is done. Such a study would be of great value to circuit designers.

3.3 Conclusion

Fabrication techniques present a challenge in two points: reliability of the process and room temperature operation (which is becoming more feasible using the newly developed methodologies). Reliability remains a problem for both the device makers who seek better and repeatable processes for implementation, and for circuit designers who try to find out new circuit ideas less sensitive to parameter variation. Co-tunneling and background charge variation are also among the causes of parameter variations. Co-tunneling can be suppressed by using several junctions in series instead of one although this may affect the speed of operation. Background charge variation remains an open area for research in two directions: better fabrication techniques to decrease this problem and new circuits which are insensitive to it.

The tunnel capacitance and conductance can be tuned to a large range of values depending on the materials and dimensions chosen. A lot of research is still needed in this area to achieve the desired values with moderate technological requirements. One such example is the newly developed SECO process.

Chapter 4

The dual-gate decimal adder

In this chapter, a decimal adder using single electron transistors as a building block is presented [77]. The design is described and the equivalent circuit is extracted, from which the DC performance of the adder is derived analyticaly. This simple approach is found to be in good agreement with simulation results. A detailed sensitivity analysis is performed in which the effects of temperature, capacitance, conductance and background-charge variations are taken into consideration and the resultant change in device performance is described. This adder needs four times less wiring than binary adders and hence alleviates the interconnections problem present in high density circuits.

4.1 Introduction

As discussed before, in the past few years several proposals were suggested for performing logic and memory applications using single electronics or quantum dots. Some of these proposals suggested using the Single Electron Transistor (SET) as a replacement for the standard field-effect transistor [14, 16], while others proposed using each electron to represent a single bit as the Single Electron Logic (SEL) [14, 31]. Others came up with even more radical ideas about the architecture and signal coupling between different parts of the circuit that should be used [33, 34, 35, 36, 37, 38, 39, 40, 41]. This was targeted to solve the wiring crisis and high power dissipation present in the previous proposals. A possible approach to solve the interconnections problem is presented here by the use of

decimal multi-valued logic. Only one wire is needed to represent a digit from 0 to 9, whereas if using binary adders four wires are needed. The problems of interconnections in digital systems in general have two facets [78]:

Edge connection As larger chips become feasible, the space for edge connections grows linearly with the edge length l, while the space for circuitry grows as l^2.

Inside the chip While the number of local modules grows as l^2, the number of interconnects in a generally connected network grows as $(l^2)!$.

A possible solution to these problems is to increase the amount of information on the interconnects between the chip's modules. As more information is conveyed, less interconnections are needed. It is also important to note that some of the design problems are essentially problems of *binary* digital design alone. This is clear from the other extreme case of analog design where interconnection complexity is *not* a problem [78].

SETs have an inherent ability to perform multi-valued operations due to their ability to "count" the charges trapped in a quantum dot and because the quantization levels for the charge are quite clear. Each step represents the addition of an extra electron to the dot. The device proposed here is a variation of the SET found in the literature, where instead of having one gate to control the charge tunneling, two gates are assumed. If the voltage between the drain and source is kept constant, the charge in the dot will be proportional to the sum of the two gate voltages which are considered as the inputs here. The use of charges to perform multi-valued logic has been proposed before using Charge-Coupled Devices (CCD) [79]. Kerkhoff and Tervoert [80] presented a small complete set of operations, while Smith [78] presented a general overview of multi-valued logic with a much richer set of operations. It may be argued that the fundamental operations needed in a computer are the addition, negation and number comparisons. Other operations can be deduced from these basic ones. The addition is considered here and a decimal base is assumed because it is the natural system humans are used to.

A schematic top view of the proposed device is shown in Fig. 4.1(a). It can be achieved using STM/AFM nano-oxidation [44, 45] or any other nanofabrication

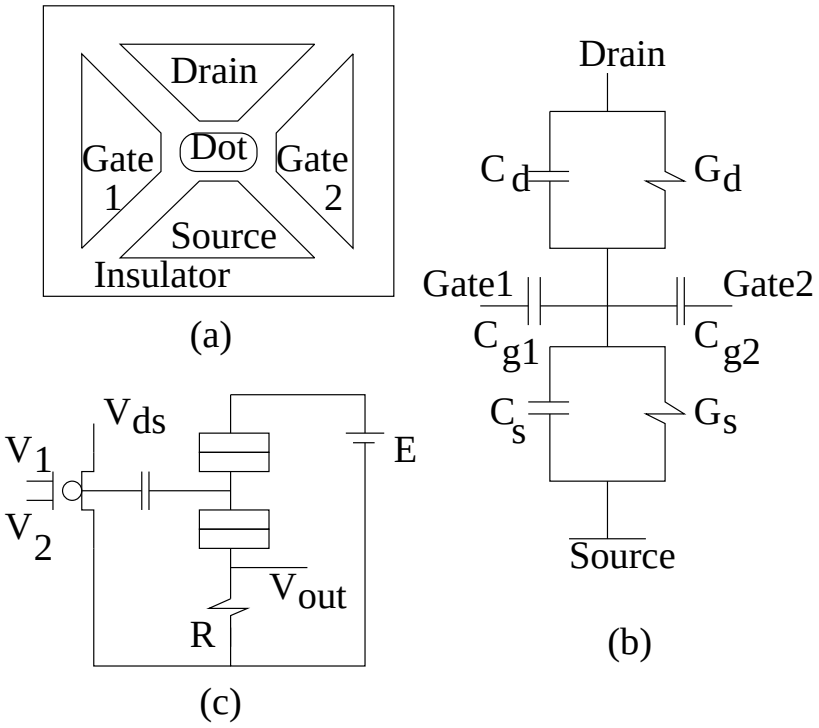

Figure 4.1: The dual-gate SET.
(a) Schematic top view.
(b) The equivalent circuit used for simulation.
(c) The device capacitively coupled to an electrometer.

technique [42, 43, 62, 63, 61]. Fig. 4.1(b) shows the equivalent circuit of the intrinsic device. The sensing of the resulting number of electrons is performed by coupling the device to an electrometer which converts the value of the charge into a corresponding voltage [20, 81] as depicted in Fig. 4.1(c).

4.2 Mathematical analysis

The analysis of the intrinsic circuit follows the same steps used for other proposals [24], i.e. drain and source voltages are assumed to be zero and only the effect of the gates is considered. Positive voltages on the gates induce negative charges in the dot, while the dot voltage, V_{dot}, induces positive charges in it. The difference, which represents the charge of electrons trapped, is $-nq$, where n is the number of electrons in the dot and q the charge of a single electron. That is

$$Q_{g_1} + Q_{g_2} = Q_d + Q_s + qn \tag{4.1}$$

where Q_{g_1}, Q_{g_2}, Q_d and Q_s represent the charge on the capacitors C_{g_1}, C_{g_2}, C_d and C_s, respectively. The energy of the circuit, E, may be written as,

$$E = \frac{Q_{g_1}^2}{2C_{g_1}} + \frac{Q_{g_2}^2}{2C_{g_2}} + \frac{Q_d^2}{2C_d} + \frac{Q_s^2}{2C_s} - Q_{g_1}V_{g_1} - Q_{g_2}V_{g_2} \tag{4.2}$$

Using the substitutions,

$$\begin{aligned} Q_{g_1} &= C_{g_1}(V_{g_1} - V_{dot}) && (4.3)\\ Q_{g_2} &= C_{g_2}(V_{g_2} - V_{dot}) && (4.4)\\ Q_d &= C_d V_{dot} && (4.5)\\ Q_s &= C_s V_{dot} && (4.6)\\ C_{tt} &= C_{g_1} + C_{g_2} + C_s + C_d && (4.7)\\ V_{dot} &= \frac{C_{g_1}}{C_{tt}}V_{g_1} + \frac{C_{g_2}}{C_{tt}}V_{g_2} - \frac{qn}{C_{tt}} && (4.8) \end{aligned}$$

the energy can be transformed to,

$$E = \frac{C_{tt}}{2}V_{dot}^2 - \frac{C_{g_1}}{2}V_{g_1}^2 - \frac{C_{g_2}}{2}V_{g_2}^2 \tag{4.9}$$

or,

$$\begin{aligned} E &= [(qn)^2 - 2qnC_{g_1}V_{g_1} - 2qnC_{g_2}V_{g_2} \\ &\quad + 2C_{g_1}C_{g_2}V_{g_1}V_{g_2} - C_{g_1}(C_{g_2} + C_s + C_d)V_{g_1}^2 \\ &\quad - C_{g_2}(C_{g_1} + C_s + C_d)V_{g_2}^2]/(2C_{tt}) \end{aligned} \tag{4.10}$$

This last form is preferred because it gives the energy in terms of the external inputs and the measured quantity n . The tunneling event occurs only when it is favorable from the energy point of view, i.e. when it causes a minimization of E. If equation 4.10 is differentiated with respect to n and equated to zero the result is found to be,

$$qn - (C_{g_1}V_{g_1} + C_{g_2}V_{g_2}) = 0 \tag{4.11}$$

The same result could be deduced from equation 4.9 where it is seen that, for a specified input voltage on the gates, the minimum energy occurs when $V_{dot} = 0$.

Table 4.1: Normalizing factors used for simulation.

Parameter	Normalizing factor
Capacitances	C_0 (implied by the user)
Conductances	G_0 (implied by the user)
Charge	q
Energy	q^2/C_0
Voltage	q/C_0
Temperature	$q^2/(k_B C_0)$
Time	C_0/G_0

That is to say that the dot voltage is increased by the gate voltages till a certain limit then a tunneling event occurs restoring it back to zero and minimizing the total energy. Assuming symmetric gate capacitances ($C_{g_1} = C_{g_2} = C_g$), the increment in the sum of gate voltages required to trap an extra electron is,

$$\Delta V \equiv \Delta(V_{g_1} + V_{g_2}) = \frac{q}{C_g} \tag{4.12}$$

This indicates that ΔV is constant, independent of the absolute voltage present on the gates, and that it is a step representing the sum of the two inputs.

4.3 Simulation results

The simulation software used [17], represents all the parameters of the circuit in a normalized form. The normalizing factors are shown in Table 4.1. This is more convenient than giving the absolute values of each parameter since all the circuit behavior is in fact scaled if the capacitances or conductances are scaled. Bearing this in mind, numerical simulations of the device performance have been performed assuming $C_g = 0.32aF$ with the scaled and absolute parameters values shown in Table 4.2. If the tunnel resistance is assumed to be $1M\Omega$ ($\gg h/q^2$), the time constant of the device is $\tau = RC_{tt} = 0.8ps$. The device itself is quite fast and —depending on its loading in a real circuit— high speed operation can be achieved.

The above mentioned values were chosen in order to have a suitable range for the input voltages since equation 4.12 predicts a voltage difference of q/C_g. So as C_g is decreased a larger voltage interval is achieved. The temperature of

Table 4.2: Values of the circuit parameters for the adder.

Parameter	Scaled value	Absolute value
C_g	1.00	$0.32aF$
C_d	0.25	$0.08aF$
C_s	0.25	$0.08aF$
G_d	1.00	$10^{-6}mho$
G_s	1.00	$10^{-6}mho$
V_{ds}	0.10	$50mV$
V_{g_1}	$0 \rightarrow 5$	$0 \rightarrow 2.5V$
V_{g_2}	$0 \rightarrow 5$	$0 \rightarrow 2.5V$
T	0.05	$\approx 300K$

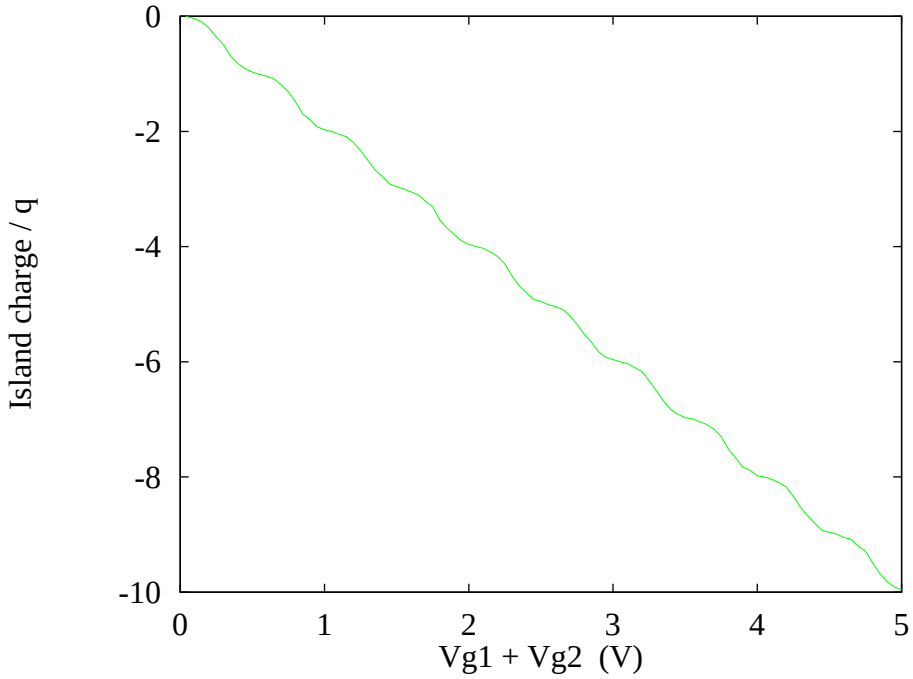

Figure 4.2: Island charge as a function of input gate voltages.

operation increases also with the decrease of the capacitance. With the choice of $C_g = 0.32aF$, the unit of voltage in the simulator is equal to $0.5V$ and a room temperature operation can be achieved.

In the simulations, the two gate voltages are swept together from 0 to 2.5V (0 to 5 units of voltage) resulting in tunneling occurring at intervals of nearly 0.5V as shown in Fig. 4.2. This is in agreement with the analytical result of equation 4.12. In the remainder of the discussion absolute values will be used and only the scope of interest in the simulation result will be displayed in the figure.

As indicated in Fig. 4.3, the increase of the drain voltage smears the characteristics so $V_d = 0.1q/C_0 = 50mV$ is chosen as the standard value. This value is

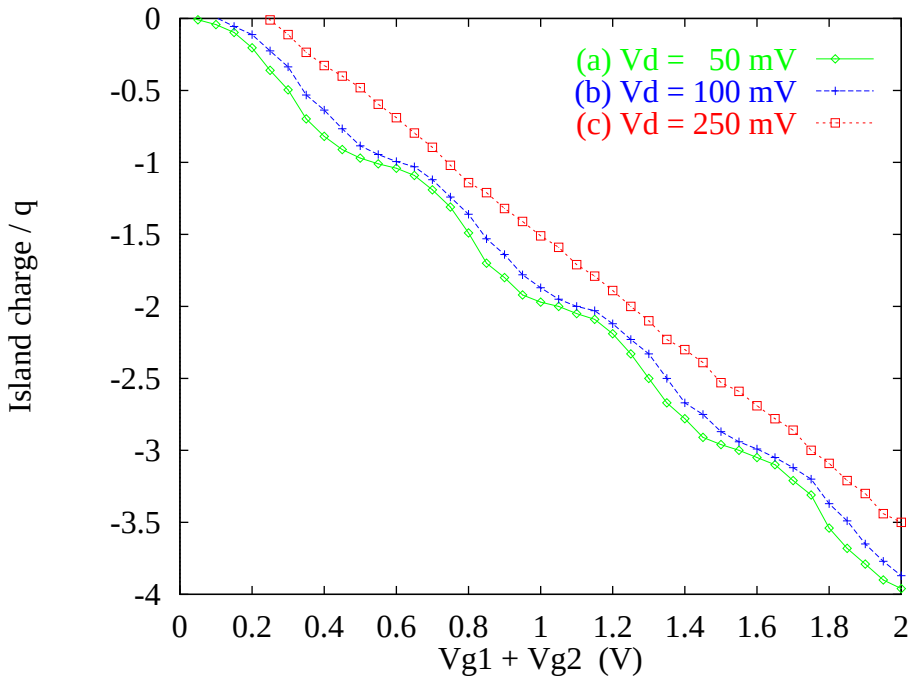

Figure 4.3: Effect of the increase of the drain voltage.

quite low compared to the gates voltages and hence validates the neglection of V_{ds} in the analytical model presented.

Another point that affects the choice of the drain voltage is the capacitive coupling between the drain and source to the dot compared to the coupling between the gates and the dot. The ratio of the source and drain capacitance to the gate capacitance is important. As this ratio is decreased as indicated in Fig. 4.4, sharper steps are obtained. Small ratios can not be achieved however since this would mean very small source and drain capacitances. That is why the ratio of 0.25 is chosen.

The sensitivity of the adder to temperature, capacitance and conductance variations has been also investigated. Fig. 4.5 shows the effect of temperature increase. Although with high temperature the steps seem to wash out, the output is still the correct value of the addition of the inputs. However, signal restoration may become a problem because of reduction in noise margins.

Fabrication tolerances can cause the thickness of the insulator between the different electrodes to vary, which leads to capacitance variation. The sensitivity

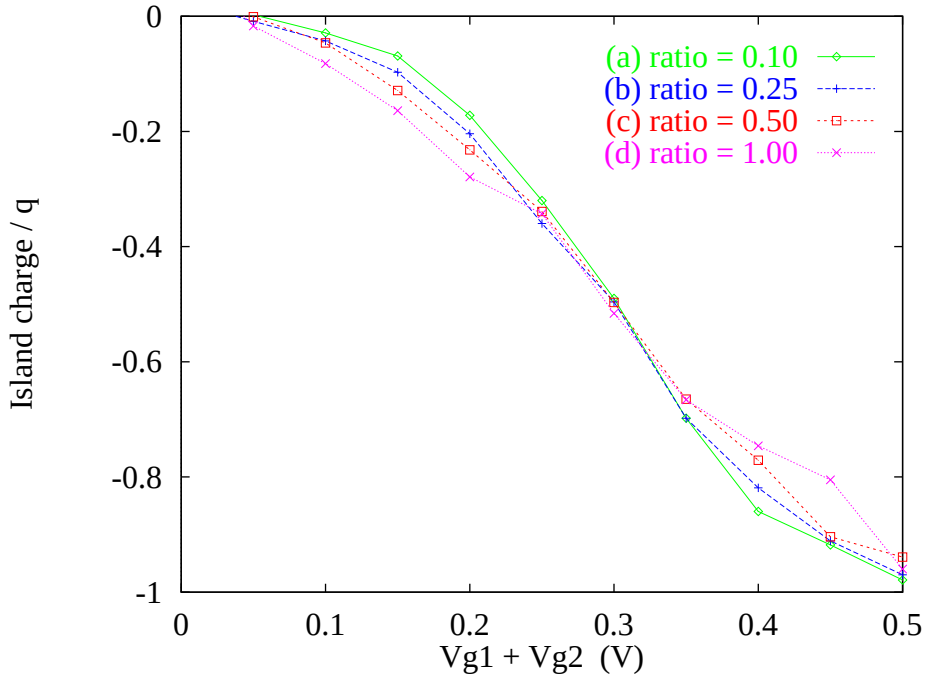

Figure 4.4: Source and drain capacitance to gate capacitance ratio variation.

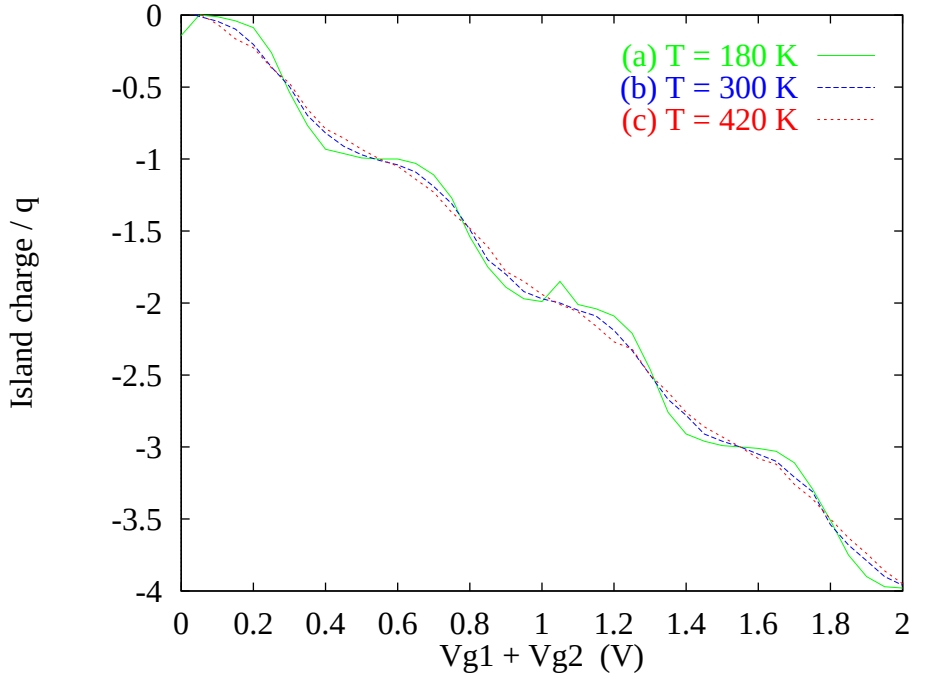

Figure 4.5: Temperature effect on the adder performance.

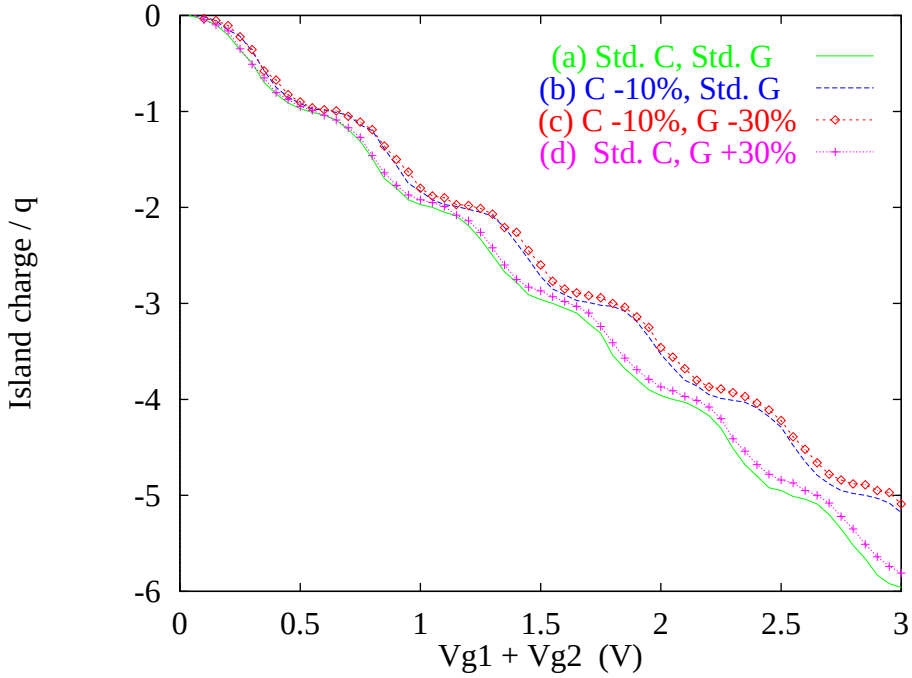

Figure 4.6: Effect of capacitances and conductances variation.

of ΔV to the gate capacitance is calculated from equation 4.12 to be

$$S_{C_g}^{\Delta V} \equiv \frac{\partial \Delta V / \Delta V}{\partial C_g / C_g} = -1 \tag{4.13}$$

This indicates that the circuit is quite sensitive to the capacitance value. Fig. 4.6 shows the numerical calculation results when all the capacitances are reduced by 10% (compare curves (a) and (b)). The predicted sensitivity of ΔV is clearly observed, manifested in each plateau increasing by 10%. This error, however, is cumulative such that when $V_{g_1} + V_{g_2} = 10$ the number of electrons in the dot is only nine.

The effect of varying the tunneling conductance, which is exponentially dependent on the insulator barrier height and thickness [71, 72, 73], has also been examined. Comparing curves (b) and (c) in Fig. 4.6, where capacitances are equal but conductances differ by 30%, it is seen that the conductance decrease has nearly no effect. On the other hand, comparing curves (a) and (d) in the same figure, a conductance increase by 30% causes the steps to gradually smear out. This may be attributed to increasing the *co-tunneling* probability, which destroys the coulomb blockade. It is important to note that, in practice, the capacitance and the conductance change in the same direction with the insulator thickness

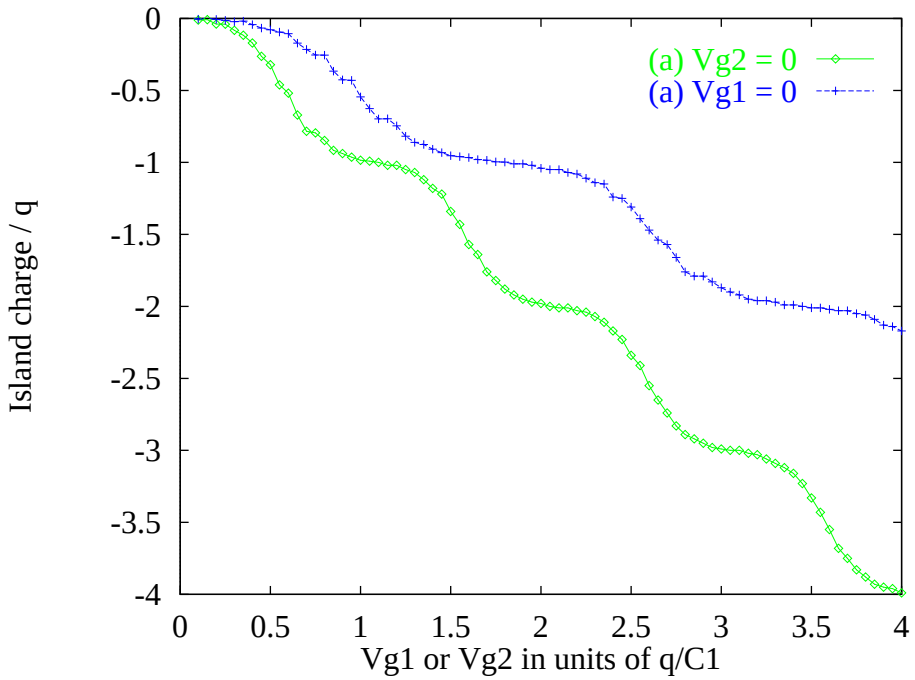

Figure 4.7: Effect of unequal gate capacitances.

variation (curve (c)).

Since a fabricated device may not have perfectly symmetric gate capacitances, this effect is investigated. Fig. 4.7 shows the results where it is assumed that $C_{g_2} = 0.6C_{g_1}$. Curve (a) is the result when $V_{g_2} = 0$ and V_{g_1} is swept, $\Delta V = q/C_{g_1} \approx 0.5V$. When $V_{g_1} = 0$ and V_{g_2} is swept as shown in curve (b) the resultant $\Delta V = q/C_{g_2} \approx 0.8$. If both voltages are swept together the voltage interval is a weighted sum of the two voltages and $\Delta V \approx 0.62$.

4.4 Discussion and conclusion

In addition to parameter variations, fabrication tolerances may induce background charge on the dot. This has a detrimental effect on the functionality of the single-island device by adding an offset to the I-V characteristics as shown in Fig. 4.8, where four random charge offsets are assumed ($-0.221q, 0.131q, 0.397q$ and $-0.372q$). The use of multiple islands is known to suppress the co-tunneling effect and the offset charges present [11]. The assumption of five islands having a random offset charge distribution (Table 4.3) results in a much more robust device since the effect of the different charges on the islands averages out to nearly zero (Fig. 4.8). The charges are chosen randomly following a normal distribution with

Table 4.3: Values of offset charges (in units of q) on the five islands.

curve 1	-0.076	0.173	-0.466	-0.268	0.123
2	0.140	0.188	-0.009	-0.020	0.800
3	0.532	-0.226	0.027	-0.221	0.131
4	-0.158	-0.451	-0.036	-0.014	0.047

mean=0 and standard deviation=$0.2q$ and the figure presents the final charge on the nearest island to the source. It is important to note that this is *not* a complete solution to the background-charge variation problem. It depends on the randomness of the charge values and polarities with respect to the specific island measured.

The presented decimal adder has an appreciable area advantage when compared to a 4 bit CMOS adder capable of performing the same function. This is mainly due to the fact that here it is a single device (in addition to another device and a resistor needed for charge sensing) which performs the decimal addition. In contrast, about 60 transistors would be needed to build a decimal adder (based on 4 one-bit binary adders). This translates into more than an order of magnitude reduction in total intrinsic device area. Since a significant percentage of the area occupancy and time delay are related to the wiring of the devices, the reduction in the number of wires results in an additional considerable advantage. It is important to note, however, that the above evaluation is based on a DC analysis and that speed comparison including loading effects has not been performed.

When this adder is compared to the ideal logic characteristics discussed in section 1.1, it is found that it fulfills the majority of the requirements at the device level except the inversion. A device for inverting the signal must be present in order to have a complete logic family. The reduction of the number of wires in this decimal adder may also increase the overall system reliability. It is, however, very vulnerable to parameter variations. Finally, it has the advantage over some of the other proposed logic elements for SETs that its inputs and outputs are all voltages. This means that it can have a fan-out and be easily interfaced with other logic elements in a large circuit with normal wires.

In conclusion, this chapter presented a decimal adder based on a single electron device where the number of active devices and wires are significantly reduced

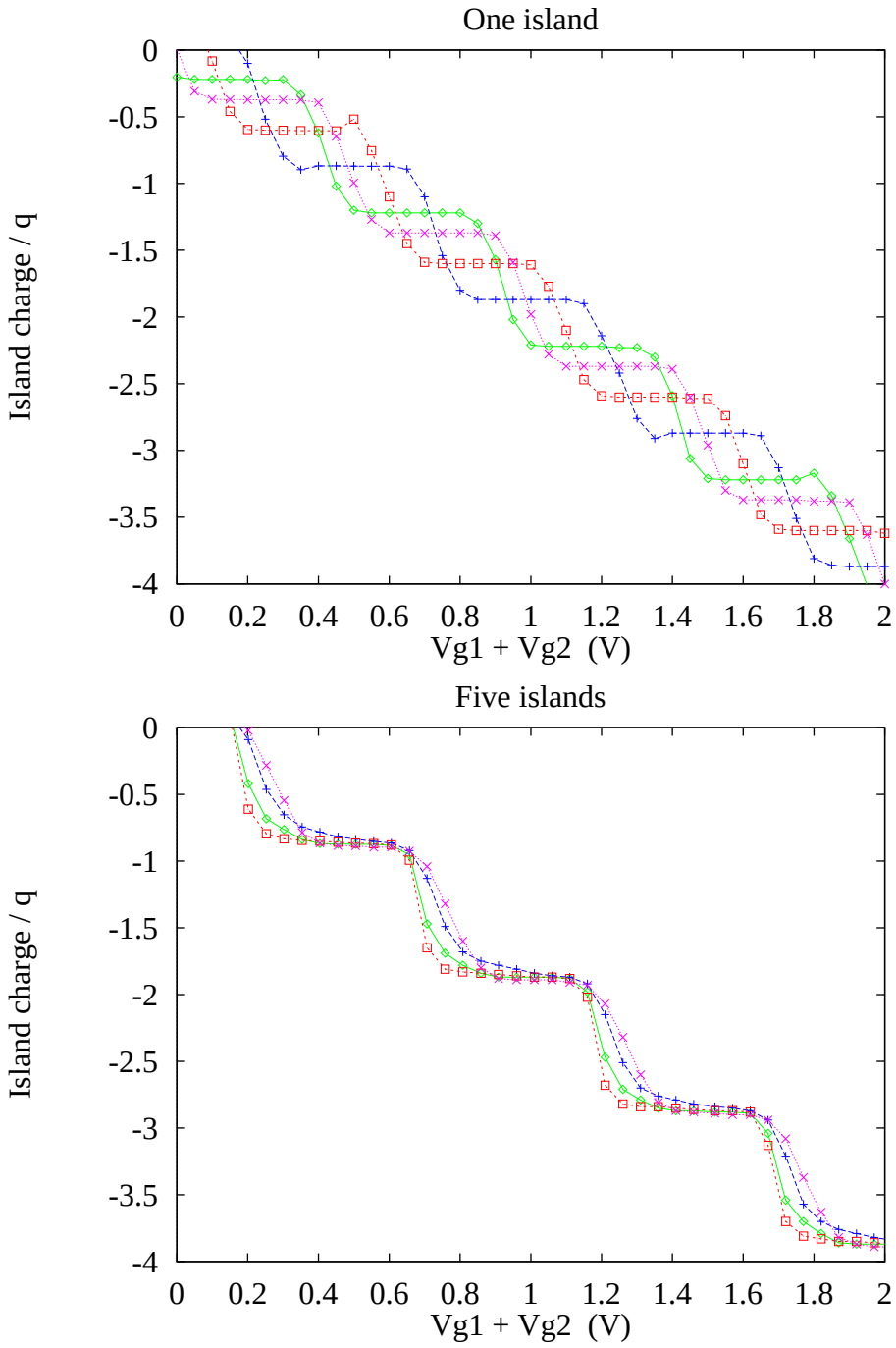

Figure 4.8: Effect of background-charge variation.

compared to conventional CMOS adders. It was found that sensitivity to parameter variations is a clear shortcoming of the decimal adder, since small changes in the design parameters and the attendant change in capacitances, conductances and offset charges have dramatic effects on the functionality of the adder. The use of multiple islands instead of only one has the potential of averaging out such fluctuations.

Chapter 5

A complete multi-valued set

The simple decimal adder presented in the previous chapter is extended here to generate a carry signal when the sum exceeds nine. Then based on this, a set of logic functions for decimal operations is developed. This set is proven to be a complete set capable of performing any decimal function.

5.1 Carry generation

When two decimal digits A and B are added the result is composed of two digits $carry$ and sum given by

	$carry$	sum
$A+B<10$	0	$A+B$
$A+B\geq 10$	1	$A+B-10$

The dual-gate adder is capable of directly giving $sum = A + B$. The carry is generated if another device with capacitances equal to one tenth the original values is used as shown in Fig. 5.1. The problem is to generate $sum = A+B-10$ when the carry is set. Fig. 5.1 presents a possible solution by the introduction of a third gate and a multiplexer whose select line is activated by the carry signal. When there is no carry a zero voltage is applied to the third gate and the result is $sum = A + B$. On the other hand when the carry is activated a voltage corresponding to the value of -10 is applied resulting in $sum = A + B - 10$.

Having more than one gate is not a big problem from the fabrication point

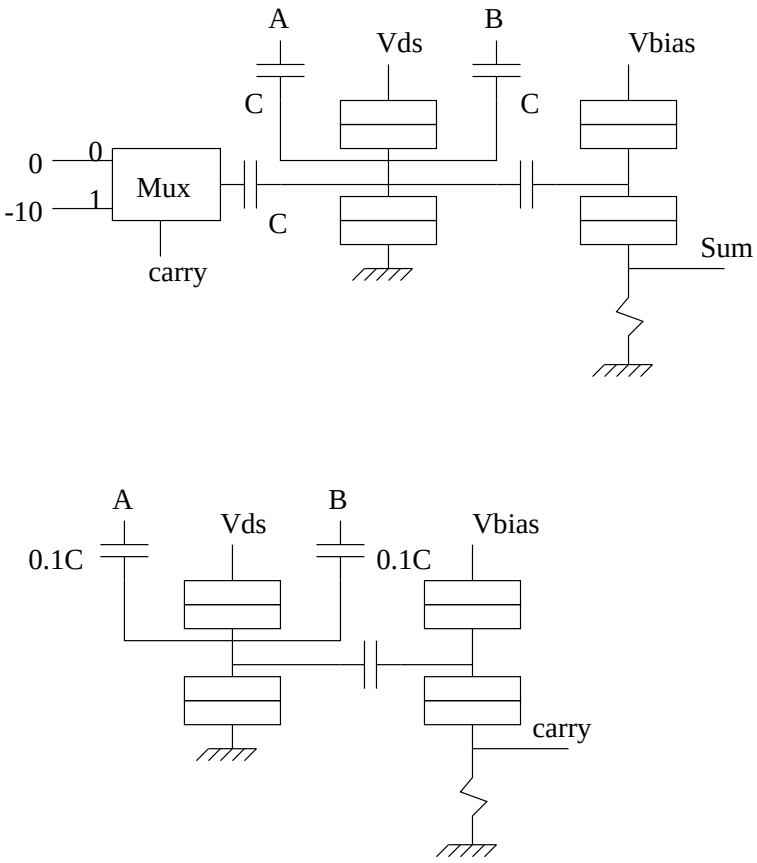

Figure 5.1: Carry generation and sum correction in the decimal adder.

of view since devices with several gates were previously reported [59, 60]. The multiplexer used must operate with multi-valued inputs. This can be achieved by using the superpass gate proposed by Deng *et al.* [82]. This gate is based on the superpass transistor presented in the same paper and constructed from a number of quantum dots and a heterostructure FET. The implementation of logic functions using superpass gates and their minimization was presented also. A less abstract approach is followed in the following sections to provide circuits that directly implement the functionality required in a computing environment.

5.2 Complement, subtract and compare

As discussed before, complementation is needed in order to have a complete logic family. For binary logic the complement of one value is just the other binary value but for multi-valued variables the complement is defined relative to the radix of the logic. In the case of decimal, the complement of a single digit A is thus defined

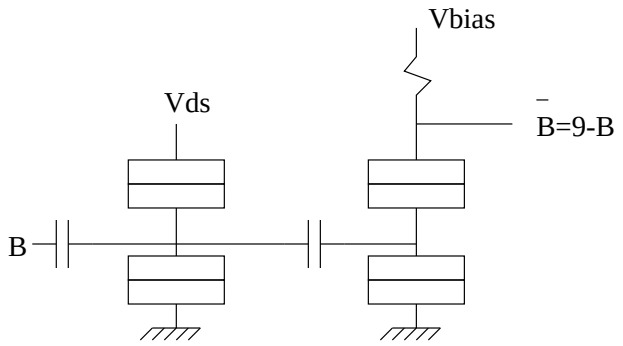

Figure 5.2: Circuit for the complement operation.

as $\overline{A} = 9 - A$. This nine's complement (radix minus one) is comparable to the one's complement in binary. To subtract the digit A from B, the complement of A is added to B. For the subtraction of a number composed of several digits the ten's complement (radix complement, comparable to two's complement) should be used. This can be easily done by performing the nine's complement of each digit and then adding one to the whole number.

Fig. 5.2 shows how the complementation can be achieved. This is the same circuit as for the adder but with the positions of the resistance and tunnel junctions of the electrometer exchanged. If for the adder the increase of the number of electrons causes an increase in current and hence an increase in the output voltage, here it causes a decrease in the voltage. By adjusting the values of the resistance and the bias of the electrometer the correct voltage levels are achieved.

The comparison and the subtraction of two digits can be performed as shown in Fig. 5.3. It is based on complement and add circuits given before. First $\overline{B} = 9 - B$ is calculated then it is added to A, the result is $9 + A - B$. If $A > B$ the carry will be 1 otherwise it is 0; this is an indication of the comparison result. The sum signal indicates the difference minus one if $A > B$ and is equal to the complement of the difference's magnitude otherwise (same as in binary implementation).

The subtract and compare operations are not the only operations that can be performed based on the adder and complement circuits. Other operations are discussed in the next section.

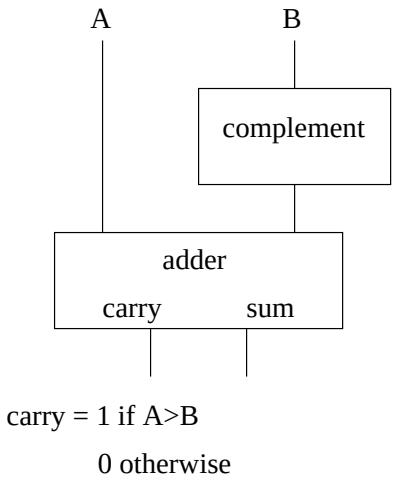

Figure 5.3: Circuit for the compare and subtract operations.

5.3 Complete set for multi-valued logic

The human reasoning is based on decimal numbers and we usually add, subtract and compare results to take different decisions in order to perform any complex operation. Also humans use binary operators to combine the results of more than one comparison. To check that $10 < x < 15$ is equivalent to a check that $10 < x$ *AND* that $x < 15$. This suggests that the circuits presented above together with the binary domain operators form a complete set of operations for decimal logic.

The basic elements that form the complete set are the multi-valued multiplexer, adder, complementer and the binary logic gates. The previous section demonstrated their use to achieve comparison and subtraction. Table 5.1 is extracted from the review paper about multi-valued logic authored by Smith [78] and it describes a large number of operations. The table is adapted for decimal values since the original is for any radix R and multiple names for the same function are removed. The variables are named x and y, while a and b denote constants.

As an example of the use of the basic set, the *maximum* function is implemented as shown in Fig. 5.4 using a comparator and a multiplexer. If x and y are interchanged the *minimum* function results.

The *successor* and *cycle* operations are performed directly by the *sum* output of the decimal adder. The *counter cycle* operation on the other hand can be done using a subtracter. The *literal* function is implemented as shown in Fig. 5.5. If instead of b, a is introduced to both comparators the *delta literal* function results.

Table 5.1: Operations on multi-valued variables.

Name	Value, condition
Restoring identity	x standardized
Complement	$\overline{x} = 9 - x$
Maximum	x if $x \geq y$ else y
Minimum	x if $x \leq y$ else y
Successor	$(x + 1)$ mod 10
Cycle	$(x + b)$ mod 10
Counter cycle	$(x - b)$ mod 10
Literal	9 if $a \leq x \leq b$ else 0
Delta literal	9 if $x = a$ else 0
Closed interval	1 if $a \leq x \leq b$ else 0
Delta interval	1 if $x = a$ else 0
Open interval	1 if $a < x < b$ else 0
Upper closed semi-interval	1 if $a \leq x$ else 0
Lower closed semi-interval	1 if $x \leq a$ else 0
Lower open semi-interval	1 if $x < a$ else 0
Upper open semi-interval	1 if $a < x$ else 0
Truncated difference	$x - a$ if $x \geq a$ else 0
Limited sum	$x + a$ if $x + a < 9$ else 9
Multiplexer	x if select=0, y if select=1
Multithreshold	use a threshold sum to look up a table
MVnor	$\overline{x}$ if $x \geq y$ else $\overline{y}$
MVnand	$\overline{x}$ if $x \leq y$ else $\overline{y}$

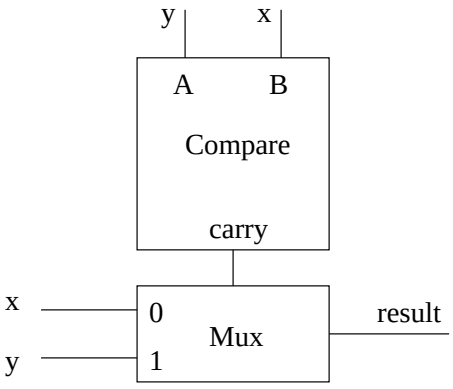

Figure 5.4: Implementation of the maximum function.

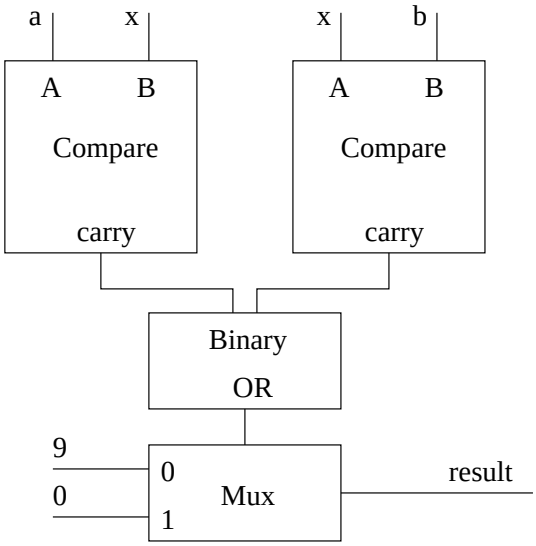

Figure 5.5: Implementation of the literal function.

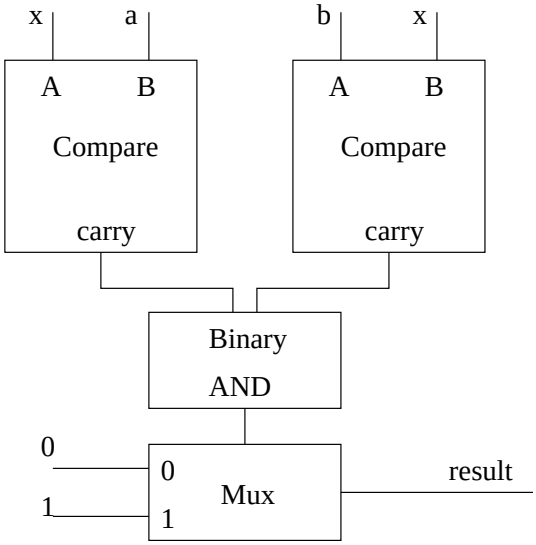

Figure 5.6: Implementation of the open interval function.

The *closed interval* is the same as the *literal* function but with 1 instead of 9 at the multiplexer input. If both substitutions are performed ($b \rightarrow a$ and $9 \rightarrow 1$), the *delta interval* is achieved.

Fig. 5.6 shows that the use of an AND gate instead of the OR gate and with a change in the order of the inputs, the *literal* function implementation is transformed to perform the *open interval* operation.

The *upper closed semi-interval* is achieved using a comparator and a multiplexer as shown in Fig. 5.7. The *lower closed semi-interval* is implemented by interchanging a and x. Also the *lower open semi-interval* is realized by swap-

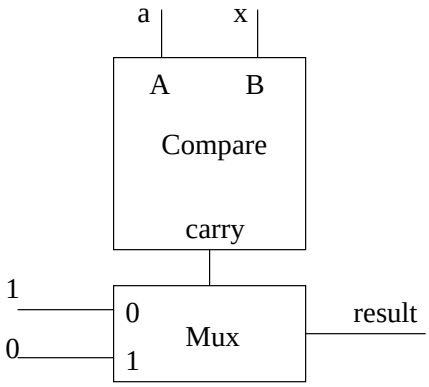

Figure 5.7: Implementation of the upper closed semi-interval function.

ping the multiplexer inputs of the *upper closed semi-interval* while the *upper open semi-interval* is realized by swapping the multiplexer inputs of the *lower closed semi-interval*.

It is clear that Fig. 5.7 is identical to Fig. 5.4 but with different inputs. The use of comparators and multiplexers is quite versatile and the reader can check that the remaining functions in the table are variations of the functions discussed above with different inputs and/or select lines. Hence, they can be implemented using the proposed basic set.

5.4 Application examples

Some real life examples are given in this section to illustrate the use of the basic elements. First a multi-digit adder is built. Then, a 1 out of 10 decoder is described and finally a multiplier is implemented.

5.4.1 Multi-digit adder

Fig. 5.8 shows how to build a 4 digit adder from the dual-gate decimal adder. A 'full adder' is first built as shown by cascading two decimal adders to add the two inputs and the carry-in signal. The block labeled B.A. (short for Basic Adder) is the initial dual-gate decimal adder without the carry generation circuit. This is enough to add the two carry signals since their sum never exceeds 9. Using this full adder, multi digit addition becomes feasible as illustrated in Fig. 5.8(b).

To add more than two numbers it would be necessary to add more digits of

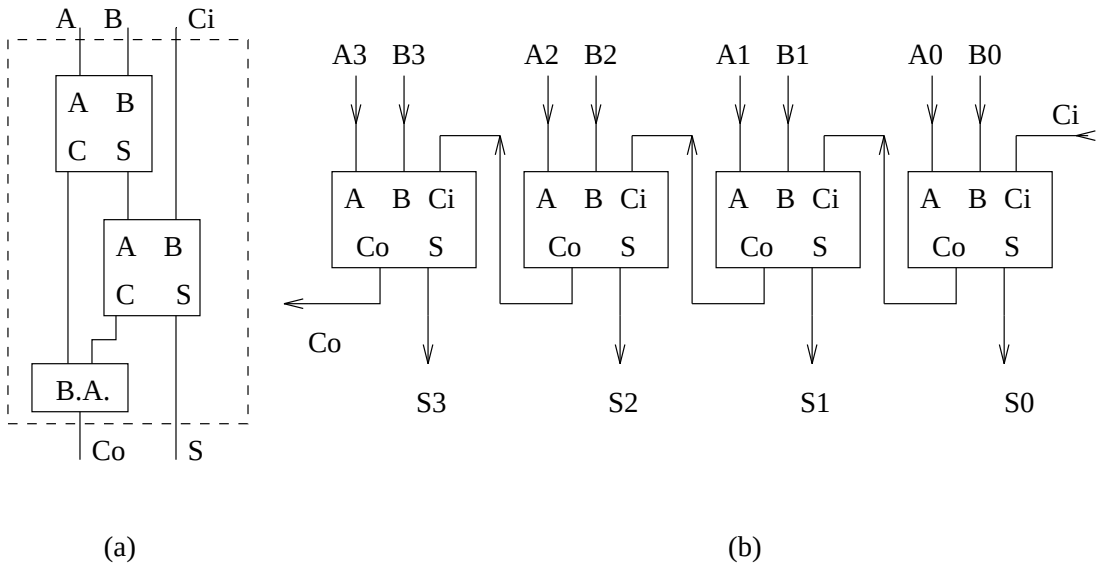

Figure 5.8: Four digit adder.
(a) 'Full adder' implementation.
(b) Connections to form a 4 digit adder.

the same weight. The use of a decimal radix allows the addition of up to eleven inputs while the output remains two digits only ($11 \times 9 = 99$). If the number of inputs is thus kept less than eleven each additional input will require the use of one decimal adder and one B.A. as shown in Fig. 5.9(a) for 4 inputs.

This serial cascading however reduces the speed of operation. A possible parallel implementation for the 4 inputs addition is shown in Fig. 5.9(b) where it is used to form a nine inputs addition block (the 4 inputs adder is enclosed by a dashed box).

5.4.2 One out of ten decoder

The implementation of a 1 out of 10 decoder is straight forward using the comparators as shown in Fig. 5.10. Outputs of the first block are either 1 for comparators corresponding to values less than the input or 0 for comparators corresponding to values greater or equal to the input.

The second block consisting of a number of binary XOR gates has only one of its outputs set to 1: the output corresponding to the initial input since this is the only XOR gate with two different inputs.

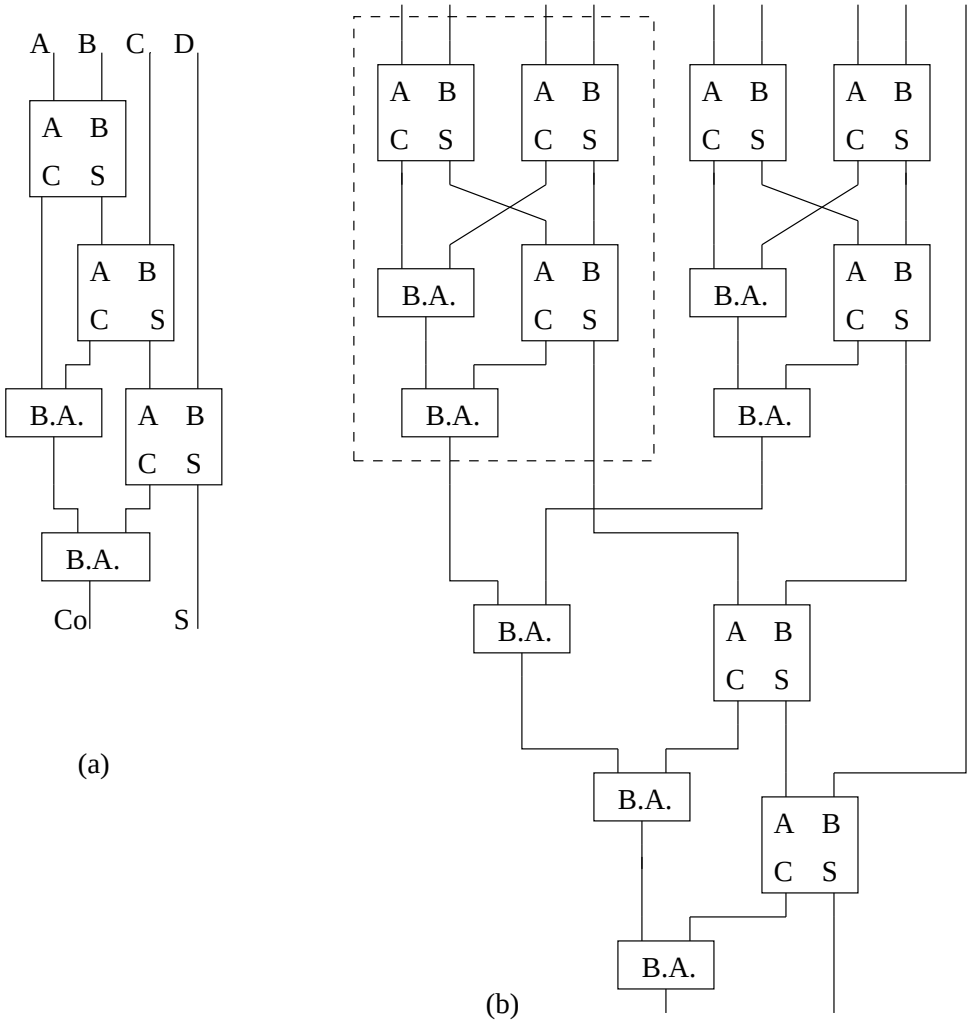

Figure 5.9: Four and nine inputs adder.
(a) Cascaded blocks to form a four inputs adder.
(b) Nine inputs adder.

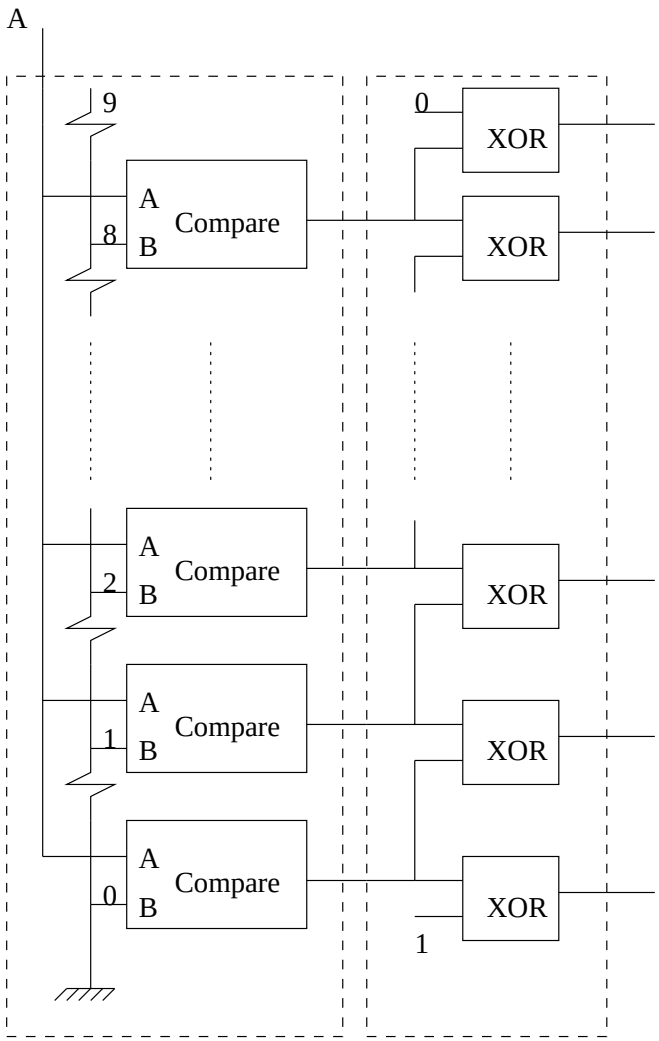

Figure 5.10: Implementation of a 1 out of 10 decoder.

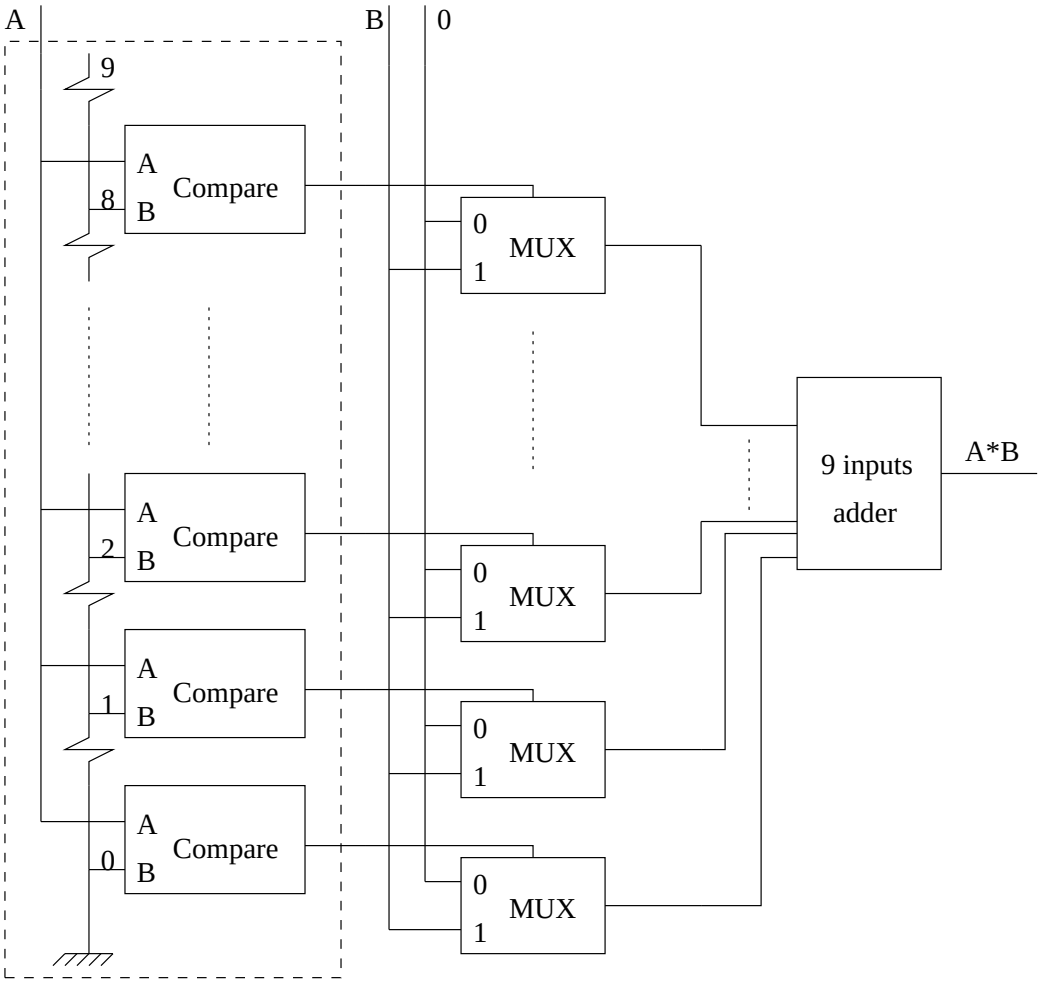

Figure 5.11: Two decimal inputs multiplication.

5.4.3 Multiplier

In the binary system, the multiplication of two bits is implemented by an AND gate. Multiplication for two decimal digits is not however that simple. It is a repeated addition of one of the digits a number of times equal to the second digit. This can be achieved by using the first block of the 1 out of 10 decoder discussed above to select the inputs of an array of multiplexers as shown in Fig. 5.11. In this configuration one of the digits (A) is entered to the set of comparators to produce a number of 1 signals corresponding to its value. These signals enable the second digit (B) to pass through the multiplexer array and we end up having a number of B's equal to the value of A while the remaining outputs of the multiplexer array are equal to 0. The nine outputs of the multiplexers can then be coupled to a nine inputs adder (Fig. 5.9(b)) to produce the final output.

This two inputs multiplier can be used to build a larger multi-digit multiplier.

It will not be described here since the intent of this section is just to illustrate the use of the basic set and not to repeat all the circuits that were built using binary logic.

5.5 Conclusion

Using the single electron adder previously presented a set of decimal operators has been built. The set, together with binary logic, is proved to be complete and able to implement any decimal function. Some examples were given to show the use of these operators in real circuits. Fabrication of such elements should be implemented in the future to validate the results given in this chapter.

Chapter 6

The dual-drain decimal adder

6.1 Introduction

Another decimal adder based on single electron transistors is presented here. Its performance and characteristics are compared to the one presented before and it is shown that this new adder may be superior to the previous one.

The previously proposed adder has tight restrictions on the parameters values and since the fabrication technology of SETs is not mature enough, it may be difficult to achieve such demands. Also the design required that the gate capacitances to the island be higher than the source and drain capacitances while there should not be any possibility of tunneling from the gates. This means that the thickness of the insulator between the gates and the island must be large enough to inhibit tunneling. A large thickness would result in a small capacitance unless it is compensated by a large area. So the gates must have a large area compared to the source and drain but must be further away. The geometric layout of a device is even complicated more when parasitic capacitances between the gates and the source and drain are taken into account. These parasitic capacitances must be minimized.

The adder presented here alleviates some of these problems in fabrication. Fig. 6.1(a) presents an SET with two drains instead of only one and with no gates at all. All the junctions are required to be tunnel junctions as shown in Fig. 6.1(b). The two drain voltages are used as the inputs and the island charge represents the summation which can be converted again into a voltage via an electrometer. The

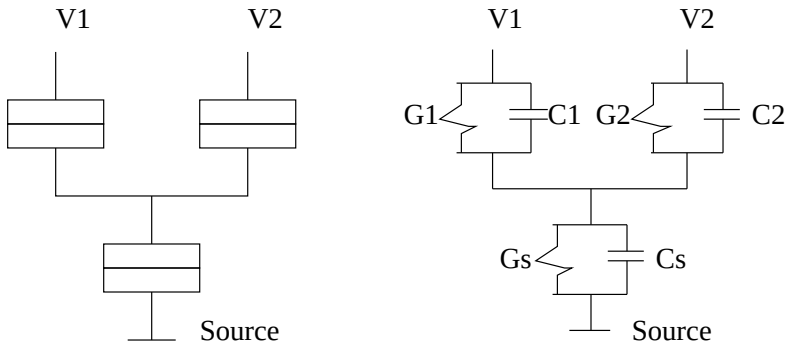

Figure 6.1: (a) Schematic of the dual-drain SET. (b) Its equivalent circuit.

operation is based on the Coulomb staircase which is a characteristic of SETs.

6.2 Mathematical analysis

The same mathematical steps of section 2.2.2 may be followed here if the Thevinin's equivalent of the two voltages and their associated capacitances is used. That is,

$$V_{equ.} = (C_1V_1 + C_2V_2)/(C_1 + C_2) \tag{6.1}$$

and

$$C_{equ.} = C_1 + C_2 \tag{6.2}$$

Assuming symmetric drain junctions, this reduces to

$$V_{equ.} = (V_1 + V_2)/2 \tag{6.3}$$

and

$$C_{equ.} = 2C_1 \tag{6.4}$$

Steps in the I-V characteristics occur thus at intervals of

$$\Delta V_{equ.} = q/C_{equ.} \tag{6.5}$$

as shown in Fig. 6.2. However, the current steps are totally smeared at high temperature.

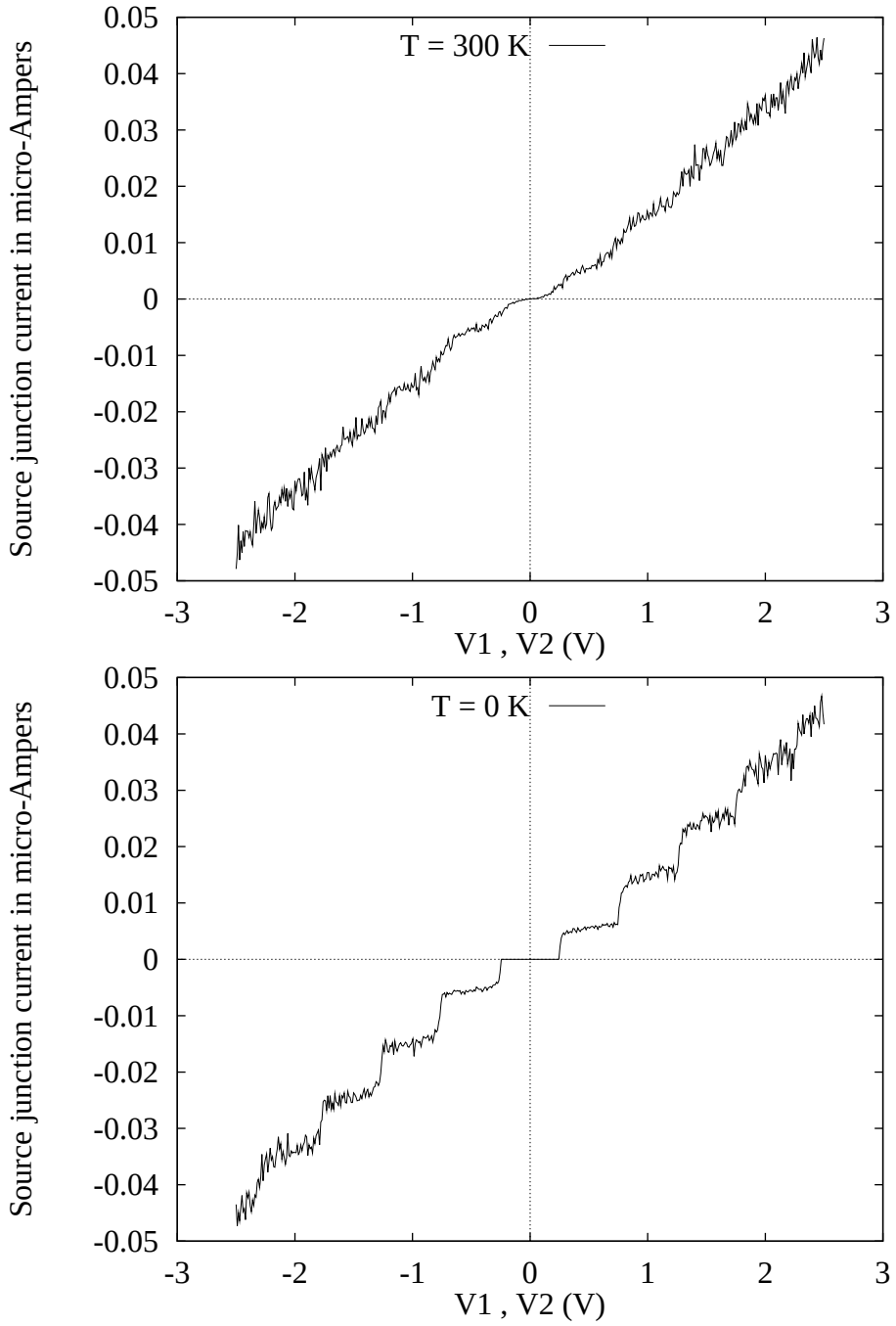

Figure 6.2: The current flowing in the source junction of the dual-drain SET.

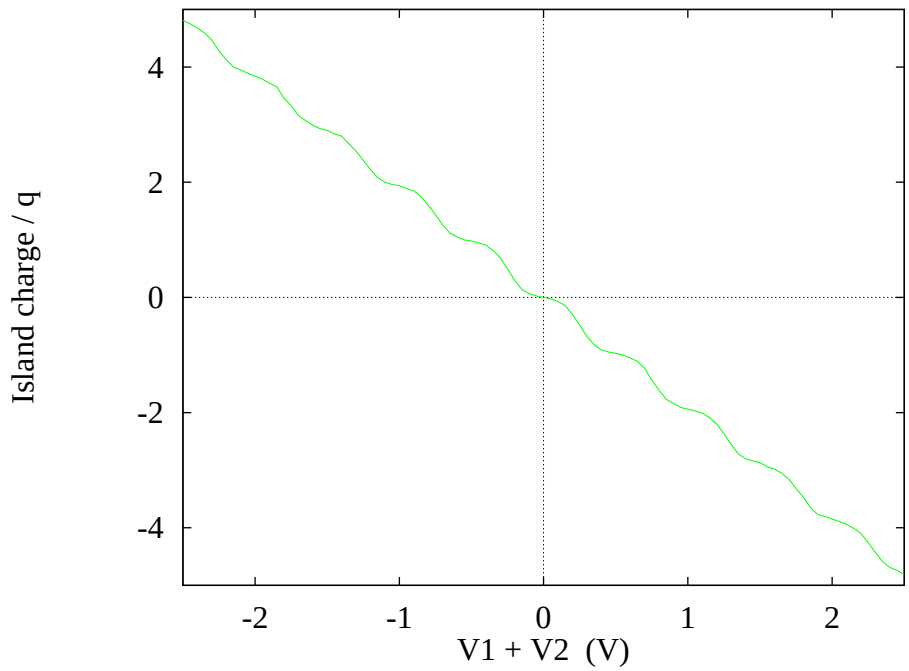

Figure 6.3: Charge on the dual-drain SET island simulated at $T = 300K$.

On the other hand, the quantization of the island's charge persists up to room temperature as shown in Fig. 6.3. That is why this charge is used as an indication of the sum.

6.3 Simulation results

Table 6.1 indicates the parameter values chosen for simulation. The two inputs are assumed to be swept together and their voltage range is taken from -2.5 to 2.5 instead of 0 to 5 as in the dual-gate adder for two reasons:

- As the drain voltage is increased the current in the device is increased and hence the power dissipation is increased. This is a shortcoming of the dual-drain adder in comparison with the dual-gate adder presented before where the drain voltage is constant and the current is not very high. By choosing a range centered around zero for the dual-drain adder power dissipation is minimized.

- At high drain voltages the current and charge steps are smeared. This will be the case specially if the device is to be fabricated using semiconductors (it happens also in metallic SETs but to a less degree).

Table 6.1: Values of the circuit parameters for the dual-drain adder.

Parameter	Scaled Value	Absolute value
C_1	1.00	$0.32aF$
C_2	1.00	$0.32aF$
C_s	0.30	$0.10aF$
G_1	0.01	$20 \times 10^{-9} mho$
G_2	0.01	$20 \times 10^{-9} mho$
G_s	1.00	$2 \times 10^{-6} mho$
V_1	$-2.5 \rightarrow 2.5$	$-1.25 \rightarrow 1.25$
V_2	$-2.5 \rightarrow 2.5$	$-1.25 \rightarrow 1.25$
T	0.05	$\approx 300K$

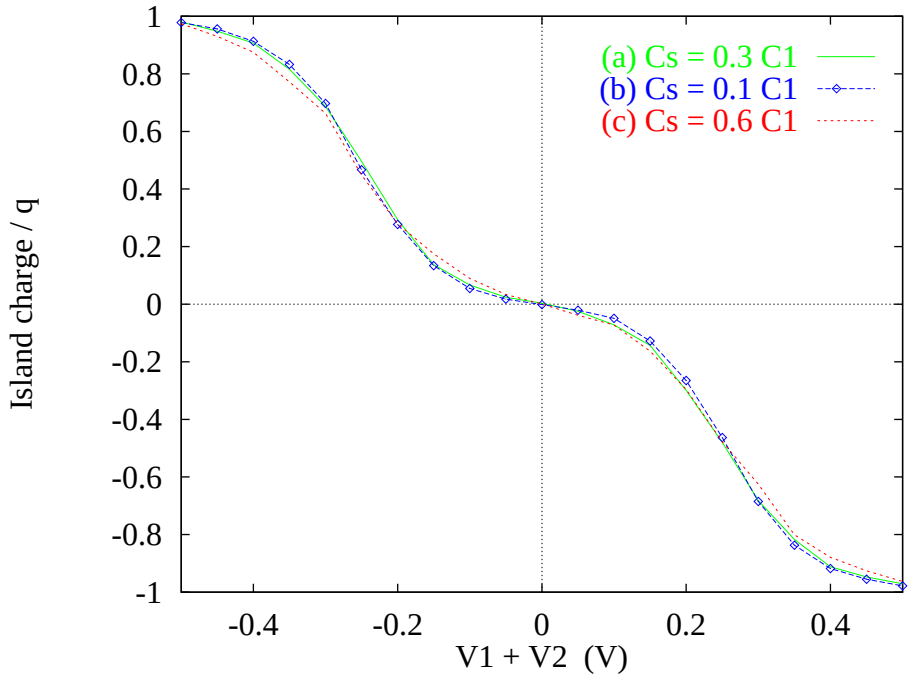

Figure 6.4: Effect of varying the ratio of drain to source capacitance.

The dual-drain adder characteristics are enhanced as the ratio between the drain capacitances and source capacitance is increased as shown in Fig. 6.4. This tolerance to the exact value of the source capacitance is important from a fabrication point of view since it means that extreme accuracy is only needed for the two drain junctions.

It is also noted, as shown in Fig. 6.5, that it is the ratio of the tunnel conductances that is important and not their absolute values (at least for low frequency operation).

The sensitivity to temperature is shown in Fig. 6.6. The device can operate at room temperature provided the capacitance values are low enough as indicated in

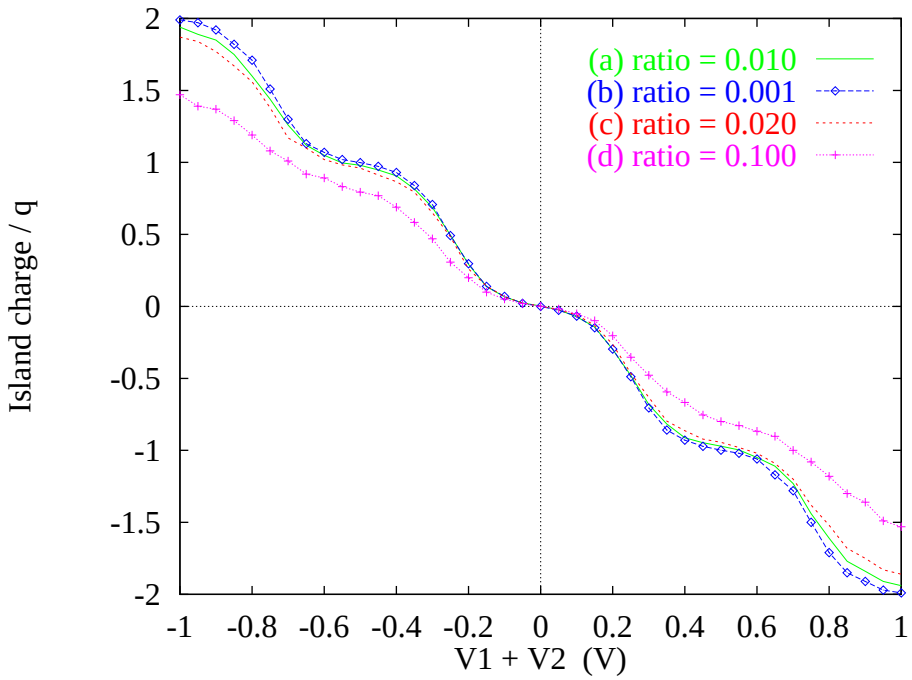

Figure 6.5: Effect of varying the ratio of drain to source conductance.

Table 6.1. As discussed before, it is only the quantization of charge that persists to high temperature and not the step structure of the I-V characteristics.

The dual-drain device is very sensitive to the absolute value of the drain capacitances. This is manifested by the direct relation between the voltage interval corresponding to one step (q/C) and the drain capacitance. Asymmetry between the junctions is also important to investigate here as was the case for the dual-gate adder. Fig. 6.7 indicates the behavior of the device when $C_2 = 0.6C_1$. As V_1 is set to zero and V_2 is swept a large shift in the characteristics occurs and steps occur at intervals of q/C_2. On the other hand, if V_2 is set to zero and V_1 swept the normal characteristics are achieved. If both voltages are swept together the steps occur at intervals related to the equivalent voltage of both inputs.

The dual-drain device is also very sensitive to any background charge present as indicated in Fig. 6.8.

6.4 Discussion and conclusion

The dual-drain adder is similar to the dual-gate adder in several features but it is superior from the point of view of fabrication. It is a decimal adder which reduces the wiring problem in a large chip, but it is also a three terminals device while

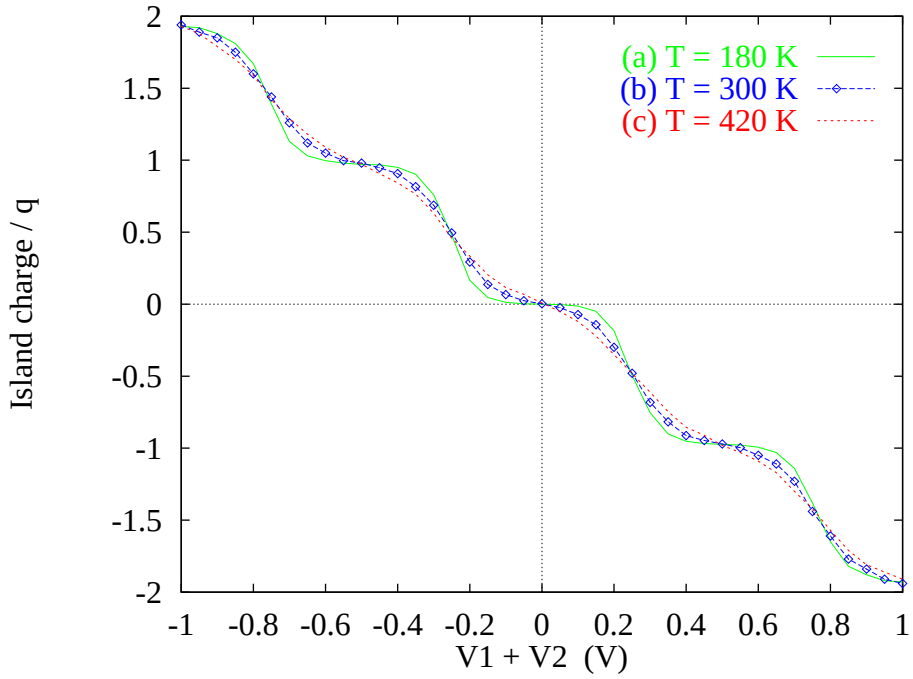

Figure 6.6: Effect of temperature on the dual-drain adder performance.

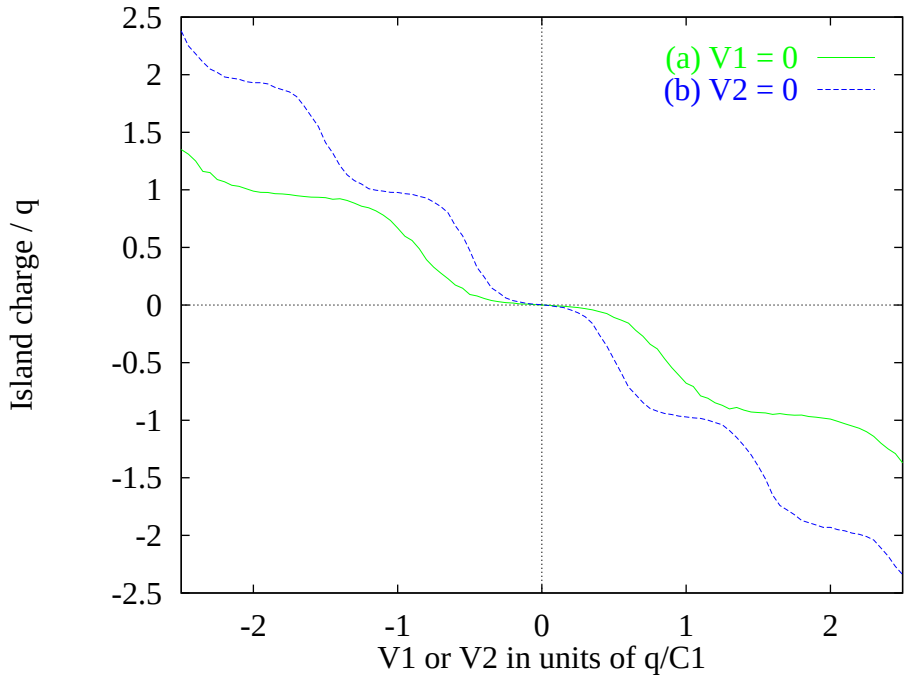

Figure 6.7: Effect of unequal drain capacitances.

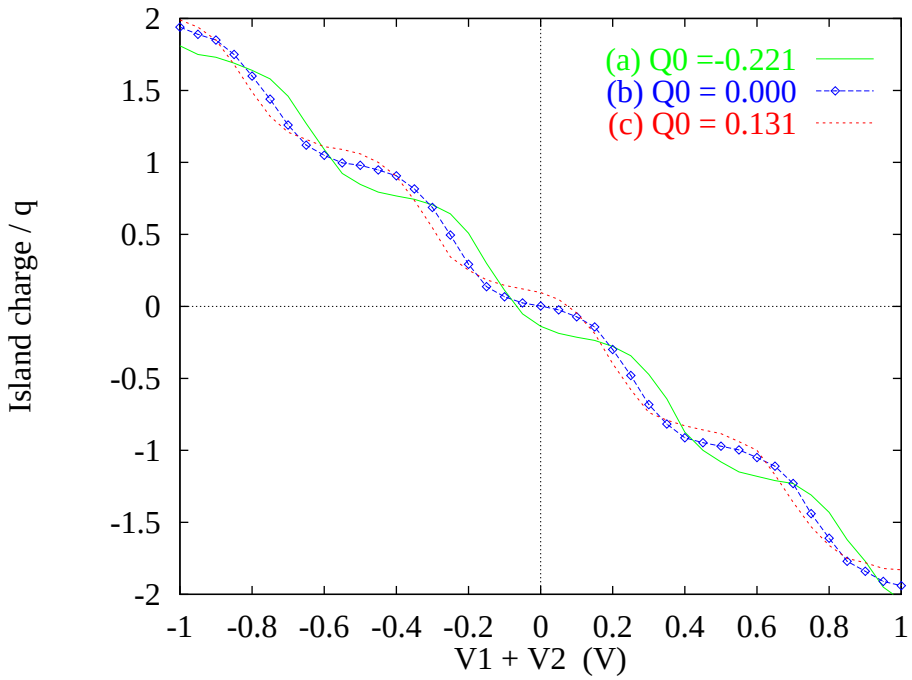

Figure 6.8: Effect of background charge variation.

the dual-gate one is a four terminals device; this alleviates the wiring problem even further. The power dissipation per device is higher in the case of the dual-drain adder but it is still small enough. The average power dissipation can be estimated from Fig. 6.2 as $P_{avg} = V_{avg} I_{avg} \approx 1.25V \times 0.02\mu A = 25nW$, while for the dual-gate adder it is $P_{avg} \approx 50mV \times 0.01\mu A = 0.5nW$.

In chapter 4 area comparison with CMOS was discussed and the time constant of the device was calculated to be $0.8ps$. When these two factors, area and speed, are combined with low power dissipation as shown here it is clear that single electron devices may become a much better choice than MOSFET technologies [50]. Single electron devices allow also the use of multi-valued logic with high radix (decimal is used here) which is not an easy task to perform with conventional devices.

Chapter 7

Conclusion

The aim of this thesis is to discuss a new technology that may be viable in the near future to overtake the role of CMOS circuits. Novel ideas are needed to solve the inherent problems present in such technology. The introduction of multi-valued logic may be one of the possible solutions and hence it was analyzed in detail.

Two implementations for the decimal adder were presented with a thorough simulation for the effect of various parameters on the operation. It is seen that, as the majority of single electron circuits, they are greatly affected by the background charge. This may be alleviated to a certain degree as was shown in chapter 4. However, background charge variation remains a challenge for circuit designers to provide circuit ideas independent of this factor. It is clear also that single electron circuits require very accurate values for the capacitances. Investigation of new fabrication methods yielding high accuracy for the parameters control are a necessity.

Besides the work needed in the fabrication and circuit design areas, a similar work is needed in the logic design and algorithms area especially if cellular automata or multi-valued operations replace the binary logic. The conventional representation of the logic value by a voltage or current signal may have to change to charges (as in the body of the thesis) or even to frequency (as in appendix B).

Whether single electron devices actually replace CMOS or not is irrelevant. The advancements that are achieved in circuits, fabrication or new logic ideas can be applied to a large number of devices. The key point is to keep on searching for solutions to the anticipated bottleneck of the electronics industry.

Appendix A

The simulation software

The simulation software used throughout this thesis is MOSES: Monte Carlo Single-Electronics Simulator. It is available for free non commercial use from Ruby Chen (email: rchen@felix.physics.sunysb.edu). It is also available in the directory /pub/moses at ftp://hana.physics.sunysb.edu .

The source code of Moses is written in Fortran and two pre-compiled versions are available, one for PCs running DOS and the other for Dec Alpha machines. I have used both versions and although the one on Alpha is much faster but it lacks the graphical output available on PCs; this forced me to use the PC version for the majority of the work. I also tried the DOS version under the DOS emulator of the OS/2 and it ran at nearly the same speed. Speed of operation is however heavily dependent on the microprocessor in the machine; it nearly doubled from a 386 to a 486 to a pentium. In general, I was able to get fast results (within a few seconds) by reducing the period length and the number of periods to cycle through in the simulation as well as the number of sweep points.

The text-based user interface is quite easy to use and I was able to run the tutorial available in the documentation and then begin my own first circuit at once. I think however that the documentation should give more examples and explain further the different capabilities of the software (specially the spectral analysis and the energy calculation).

Only voltage sources, having all the same AC period, are allowed in Moses. I think that it would be beneficial if this restriction is removed by allowing different periods and different phase angles for the different sources as well as allowing the

use of current sources. This would ease the simulation of turnstiles, pumps and the SET oscillations. Another feature that is missing in Moses is hierarchy. It does not allow the use of previously simulated circuits as building blocks for new circuits. Adding a single junction to the circuit design means re-entering the whole circuit again to the program.

Despite all these comments, this first version of Moses is capable of satisfying the needs of a lot of users as it did to me. I am grateful to Ruby Chen and the single electronics group of the state university of New York at Stony Brook, without Moses I would have not been able to accomplish my work.

I am including here a description of the algorithm used in Moses so that the reader can appreciate what the software does. This description is a part of the file "changes.doc" available with the source code.

```
Sketch of the algorithm for one run:

1. Cycle through as many periods as specified in the
   time parameters.

   For every cycle:

    a. For every time step of the cycle:
       1. Display motion picture text results.
       2. Calculate the potentials of the nodes, by
          taking linear combinations of the potentials
          on the nodes due to external potentials and
          island charges.
       3. Calculate the tunneling rates gamma(i,j)
          between each pair of nodes according to the
          "orthodox" theory.
            gamma(i,j) = {G(i,j)*dW(i,j)/(e*e)} /
                                 {1-exp[-dW(i,j)/k*T]}
           where
               G(i,j) is the tunnel conductance
```

between nodes i and j,

dW(i,j) is the energy change from

one charge tunneling,

k is the Boltzmann constant and

T the temperature.

Energy changes are found from the potentials and elements of the capacitance matrix.

4. Check for Coulomb blockade. Coulomb blockade is said to occur if

gamma_sum < 1E-30

where gamma_sum is the sum of tunneling rates across all junctions.

5. If no Coulomb blockade, simulate a tunneling event:

-Generate a random number between 0 and 1 for the probability P of a tunneling event. Convert this to a tunneling time delt:

P = exp[- gamma_sum * delt]

If this time is less the time step then a tunneling event occurs. In the accelerated DC run option, the tunneling time is not random, but equals 1/(gamma sum).

-Generate another random number (uncorrelated to the first) to find where the tunneling event occurs. The probability for the tunneling event to occur through a given junction is equal to the junction´s tunneling rate divided by gamma sum.

6. Update the time:

- If system is Coulomb blockaded, and all external signals are static, and there is no charge transfer through the resistors,

increment time to the end of the final cycle.

- If a tunneling event occurs, increment the time by the tunneling time delt
- Otherwise, increment the time by the time step.

7. Update spectral density variables (see below).
8. Update time-weighted sums of potentials and charges for statistics calculations.
9. Calculate change in island charges due to Ohmic resistors. Contributions are current flow and Nyquist noise.
10. Proceed with next time step.

b. Update variables for calculating errors:

- time-weighted sums over cycles of squares of potential and charge time-averages.
- sum over cycles of squares of net number of tunneling events.
- time-weighted sums over cycles of average current.

c. Proceed with next cycle.

2. Final line of motion picture text.

3. Finish calculating statistics:

- time-average charge, potential and current
- cycle-average net number of tunneling events
- errors

4. Plot results on screen

See also

K.K.Likharev, N.Bakhvalov, G.Kazacha and S.I.Serdyukova,

IEEE Trans. Magn.25, 1436 (1989).

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Appendix B

Analog ideas

Although the emphasis through out the thesis is on digital circuits using single electron devices, some analog ideas are presented here without full analysis.

B.1 Frequency shifting

A brief discussion of the turnstiles was given in chapter 2. It was shown that the output current is related to the input voltage frequency by the relation $I = nqf$. During each cycle n electrons pass through the device where n depends on the DC offset and AC amplitude of the applied signal (refer to Fig. 2.8). If these parameters are chosen so that $n = 1$, the relation becomes $I = qf$. But the dual relation $f = I/q$ is also present in the SET. If a constant current passes through an SET the voltage across it oscillates at the indicated frequency. The idea presented here is to combine both effects in a single circuit as shown in Fig. B.1.

According to the node equation the total current I is equal to the sum of $I_1 = qf_1$ and $I_2 = qf_2$ i.e.

$$I = I_1 + I_2 = q(f_1 + f_2) \tag{B.1}$$

This is a constant current passing through an SET, hence the voltage across it oscillates at a frequency

$$f = \frac{I}{q} = f_1 + f_2 \tag{B.2}$$

The current flowing in a turnstile must be independent of the voltage applied

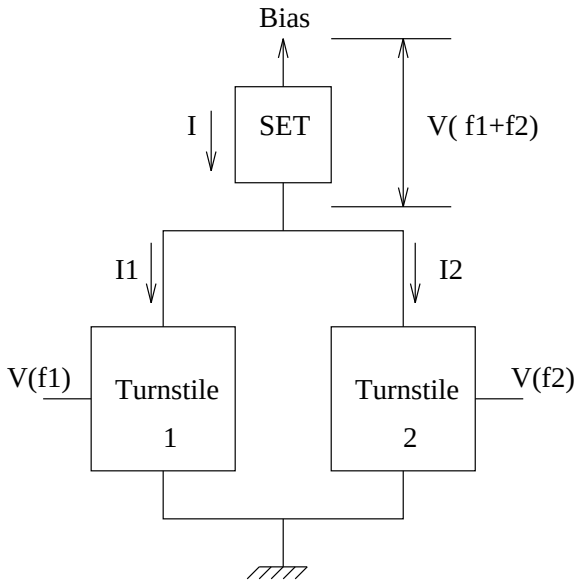

Figure B.1: Proposed frequency shifter/adder.

across it for correct operation of such a circuit. Experiments indicate that such current plateaus are seen [20]. Simulations also indicate this behavior as shown in Fig. B.2. Due to the simulator restrictions both input frequencies are set to the same value $f_1 = f_2 = 1/100RC$ (R is the tunnel resistance of the junction and C its capacitance) giving currents of $I_1 = I_2 = q/(100RC)$ as indicated in the figure. The total current is shown also which is the double of the turnstile currents. This validates the basic concept.

Unfortunately, the spectral analysis algorithm available with the simulation software does not handle turnstiles and pumps accurately. Other simulators [53] may give better results, however the final test would be to fabricate such a circuit and test it with real inputs. If it does perform the frequency shifting function then it can be used in communication circuits instead of the currently used mixers which are nonlinear elements producing signals with high harmonic content. A detailed study of the total harmonic distortion of the output in the proposed circuit is necessary to have a fair comparison. It should be noted that Fig. B.1 shows a circuit that shifts the frequency up, if shifting down is required then the position of the two turnstiles with respect to the SET must change. If the position of the first turnstile is interchanged with the SET the current equation becomes $I = I_1 - I_2$ resulting in $f = f_1 - f_2$.

This frequency shifter/adder can also be used in digital circuits —whether

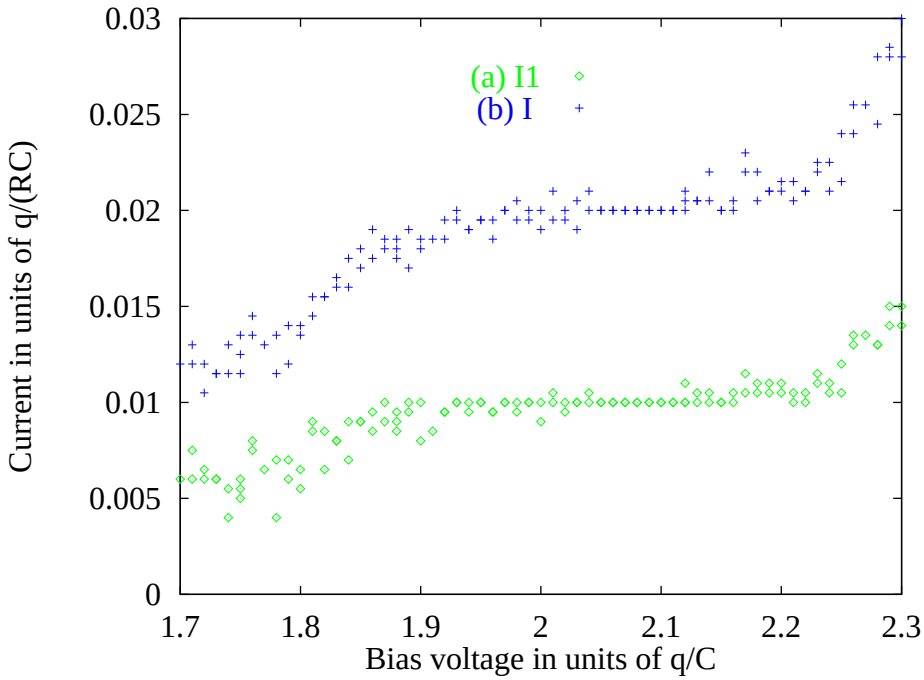

Figure B.2: Simulation results of the frequency shifter/adder.

binary or multi-valued— by assigning a certain frequency for each logic value instead of using a voltage level for each value in conventional circuits. A main advantage of such a notation is that the frequency spectrum is large and wide gaps between the different frequencies can be used which may result in wide noise margins.

B.2 Frequency modulation

The SET relation $f = I/q$ can be used also to perform frequency shift keying (FSK) or frequency modulation (FM) when the current is considered as the input signal and the voltage across the SET as the output signal.

FSK can be implemented by coding the input bit stream into two different current levels I_1 and I_2. If the bit duration is long enough compared to the time constant of the SET junctions, I_1 results in an output voltage with frequency f_1 and I_2 gives f_2. This is a direct implementation of FSK. The same concept applies to produce FM, the only difference is that the current is a continuous variable in this case. Its frequency of variation must remain however very small compared to the time constant of the junctions.

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(email: rchen@felix.physics.sunysb.edu) or in the directory /pub/moses at ftp://hana.physics.sunysb.edu.

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