Complete Logic Family Using Tunneling-Phase-Logic devices

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Abstract

This paper presents the work done to develop and characterize the behavior of binary Tunneling Phase Logic (TPL) devices. Three input NAND, NOR and MINORITY functions are demonstrated using a *single* TPL element. The fan-out of the gates is discussed as well as the loading effects of multiple gates in cascade. Stable regions of operation are reported and future research possibilities are explored.

1 Introduction

The majority of digital circuits use voltage levels to indicate the different logic values. Beside the voltage, current-mode, charge-mode (like Charge Coupled Devices [1, 2] or Single Electron Logic [3, 4]) and phase-mode [5] circuits also exist but are less popular. The use of the frequency of a waveform [6] or the use of its phase with Tunneling Phase Logic (TPL) [7] were recently proposed based on single electron devices. Single electron devices are viewed as the most promising approach for replacing CMOS to achieve terascale integration and low power density (although the total chip power may still be high due to the large packing density.)

The use of the phase of a waveform to represent logic values in digital circuits was proposed a few decades ago [8]. Two-phase (binary) and three-phase (ternary) logic using TPL have been recently analyzed as well [7, 9]. However, circuit and logic gate design issues are not yet well understood. The previous work for the binary case was restricted to an unloaded gate (mostly with a single input to work as an inverter) to study the fundamental basis of operation. In the current work, the loading effects on 3 input gate has been studied as well as the possible logic functions which turned out to be versatile enough to form a complete logic family. The goal is to have a better understanding of TPL gates used in binary logic circuits and how they can be employed to build terascale systems and applications.

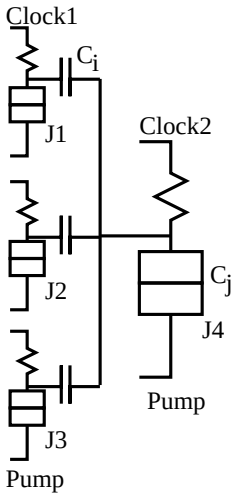

Figure 1: Basic TPL gate driven by three similar gates.

The single TPL is assumed to have several capacitively coupled inputs and to feed into some load capacitance. It was found that, within a certain parameter range, the 3 input-2 phase TPL of Fig. 1 implements the inverted majority function (minority function) of its inputs [7]. This means that if two of the inputs have opposite phases, they will cancel each other and the remaining one will get inverted by the TPL. If all three are the same the TPL will just give the inverse.

2 Discussion and simulation results

The simulation reported here were performed using the *st* package written by F.Y.Liu. The package implements a Monte Carlo simulation of single electron tunneling [10] and is similar to the popular *MOSES* simulator, but it has an easy way of specifying the circuit and its stimulus. It takes a spice file format and produces a text file with the required output values versus time. The output can be then plotted using any graphic program.

A new set of capacitance values as well as bias points have been explored in the present work. First, the tunneling junction capacitance (C_j) was normalized to a value of 1.0 and the resistance to a value of 1.0. The simulations were done for the ideal case of zero temperature with a finite but large tunneling conductance G_T ($G_T \gg 1/R$) to examine the idealized case of low tunneling jitter. In *st*, the charge is normalized to that of an electron (q) and hence the voltages are measured in q/C and the time in $C/G = RC$. A sinusoid is used for the pump and the clock is a step function whose rise time is 0.1 of the pump cycle. Both have an amplitude of 1.0. As a first step, the interconnection capacitances were varied over a wide range with $C_j = 1.0$. It was found that stable binary operation was not possible unless very low values are used (which means the inputs are not strongly coupled to the gate). It was clear that the overall capacitance linked to each element and specially C_j is too large for binary operation. A systematic reduction of C_j by a step of 0.1 was then carried out while keeping the interconnection capacitances at a value of 0.01 to lower their effect. At $C_j = 0.7$, stable binary locking was achieved. Similarly, the values of 0.6 and 0.5 gave binary operation while a value of $C_j = 0.4$ resulted in ternary locking.

With $C_j = 0.5$ and $C_i = 0.01$, the amplitudes of the pump and the clock were varied together. Increasing both from 1.0 to 1.1 introduced more noise into the output while increasing them to 1.2 caused the devices to go out of the locking range. Decreasing both of them to 0.9 caused the circuit to run into a ternary mode of operation. It was assumed that a ratio of 1 to 10 between C_i and C_j is more appropriate to get a stronger coupling between the inputs and the gate. Hence, the values were set to $C_j = 0.5$ and $C_i = 0.05$ for the following simulations. In this case, the range for binary operation when the pump and clock amplitudes were varied together was shifted down to $0.9 - 1.0$ from the $1.0 - 1.1$ discussed above for the case of lower C_i.

Since the pump is driving the whole chip, reducing its amplitude is of prime importance for power reduction. A set of other simulations were performed to check the possible pump amplitude range. Results for a gate configured as a MINORITY with inputs set to 000 are shown in Fig. 2. The amplitude of the clocks is set to 1.0 and the values for C_j and C_i are 0.5 and 0.05, respectively. Clock1 is turned on at time=0 and remains on until time=23. Clock2 is turned on at time=11 and remains on through the end of the simulation at time=90, representing 135 pump periods. During the clock overlap ($time = 11 \rightarrow 23$), junction $J4$ locks in the '1' state consistent with MINORITY function and remains in this state after clock1 is turned off for the range of pump amplitudes(V_P) from $V_P = 0.5$ to $V_P = 1.1$. This represents the correct operation. Different failure modes are also shown in the figure. The top most ($V_P = 0.2$) does not lock into the correct phase when the inputs are applied to it. The gate functions correctly for the two values shown in the middle of the figure ($V_P = 0.6$ and $V_P = 0.9$). For $V_P = 1.2$, which is the fourth from the top, the junction $J4$ locks to the correct state but then once the inputs are turned off at $time = 23$, it flips to the opposite state. As for the bottom most curve shown with $V_P = 1.5$, the junction does not run in binary mode after the inputs are turned off.

The next parameter checked is the instant at which the clock rises with reference to the pump cycle, which can be called "phase of the clock". Since the circuit is operated in binary mode, it is needed to check the effect of the clock phase over two pump cycles (the duration of one input signal). The results are shown in Fig. 3 where the horizontal axis is the instant at which the clock starts to rise shown as a fraction of a pump cycle. Results are shown for two successive cycles N and $N + 1$. The vertical axis presents the effect of the variation of C_i. A choice of $V_P = 0.9$ is made for the pump amplitude and 1.0 for the clock amplitude. With higher values of C_i, the operation is that of a MINORITY gate, while at lower values, the functions become much richer including NAND, NOR and

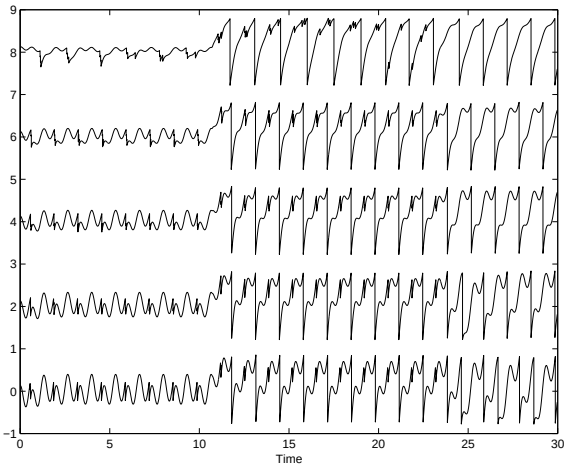

Figure 2: Voltage across junction $J4$ as a function of time for different values of pump amplitude V_P. The curves are offset for clarity and from top to bottom, $V_P = 0.2, 0.6, 0.9, 1.2, 1.5$.

MINORITY. The clock can control the operation as if it is a programmable gate.

The fan-out capabilities for the 3 input gate configured as a MINORITY was also examined. Since it is clear that the total capacitance connected to the gate has an effect, the influence of C_i was studied for the case where $C_j = 0.5$ It was found that fan-outs of 1,2 and 3 are possible for C_i equal to $0.05, 0.04$ and 0.03 respectively.

3 Conclusion

An analysis of a 3 input binary TPL gate has been presented. It was shown that NAND, NOR and MINORITY functions can be obtained in a single element. Within a certain range of coupling capacitance, only minority function is obtained, while under other ranges all three functions can be selected by using the clock phase as a control signal. The fan-out capability of the gate was also found to be dependent on the coupling capacitance, with fan-outs as high as 3 being possible in some cases. While the useful parameter ranges obtained thus far are small and the effects of thermal noise and tunneling jitter have not been considered, these results show that a complete programmable logic family can potentially be obtained using TPL gates.

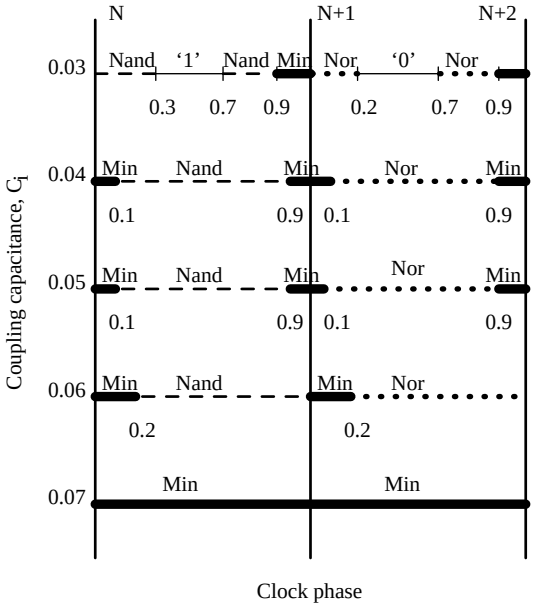

Figure 3: Clock phase and capacitance effect on the logic function. Results are shown for two successive periods starting after an even number of cycles from the start of simulation time.

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