An Adder for a Redundant Digit Arithmet

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General Outline

- Time delays in floating point addition
- Proposed system
- Modeling and comparisons
- Simulation results

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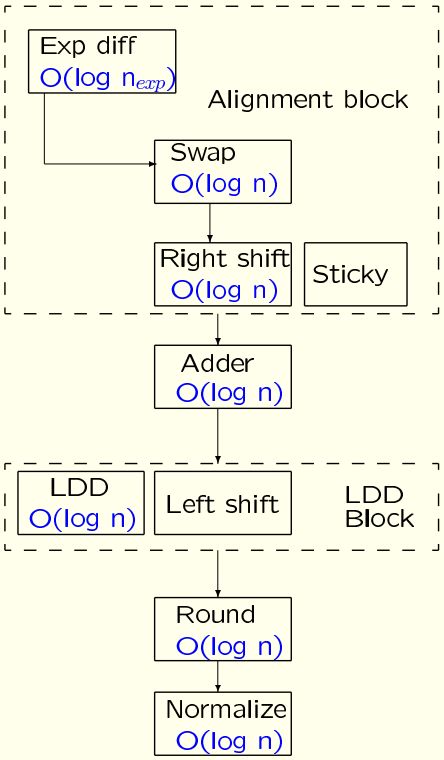

Time delays in the blocks of an adder (one-path

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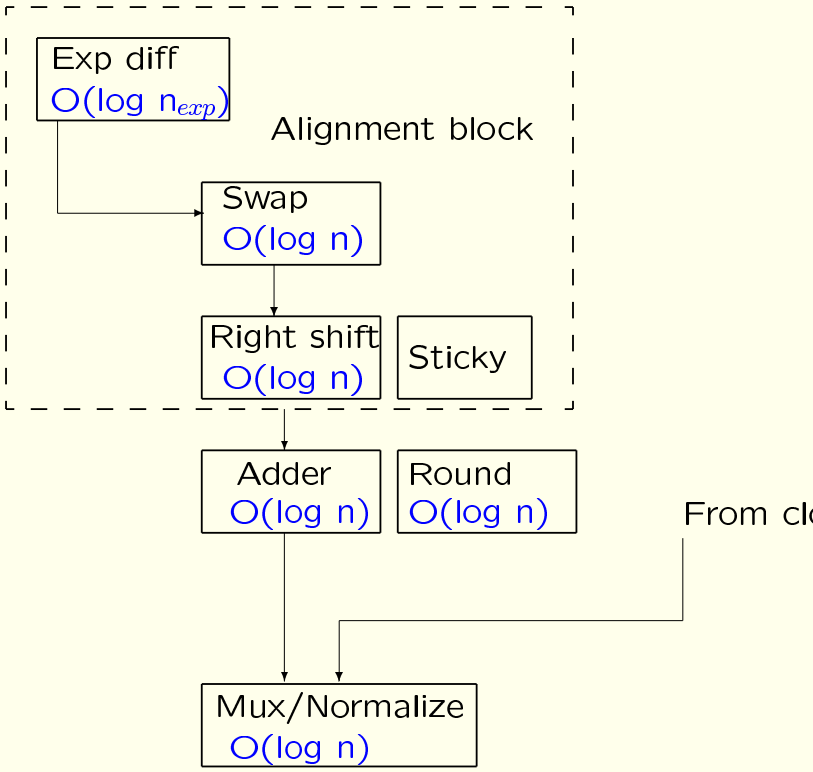

Time delays in the blocks of an adder (two-path

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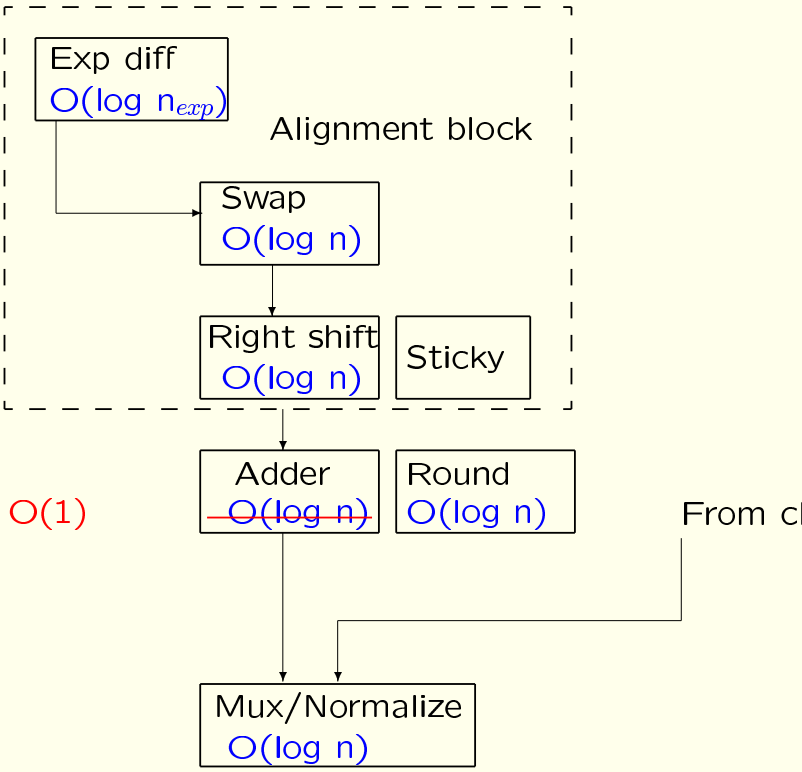
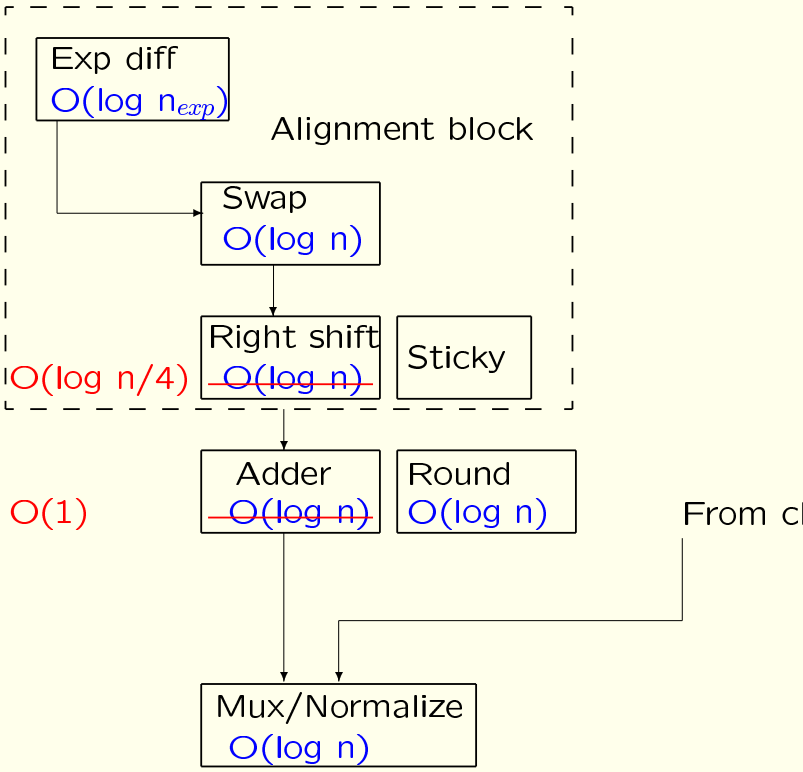
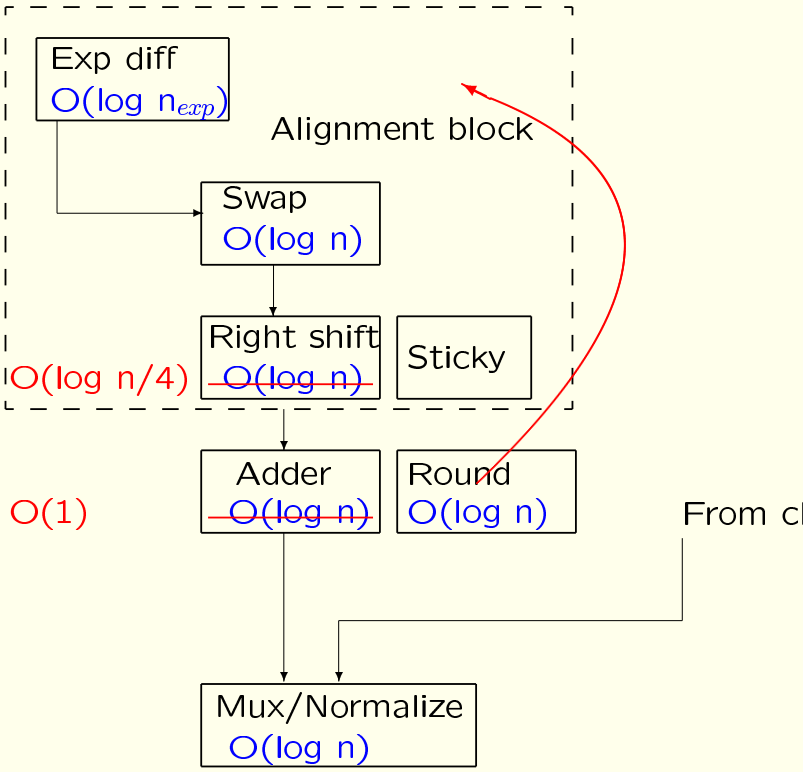


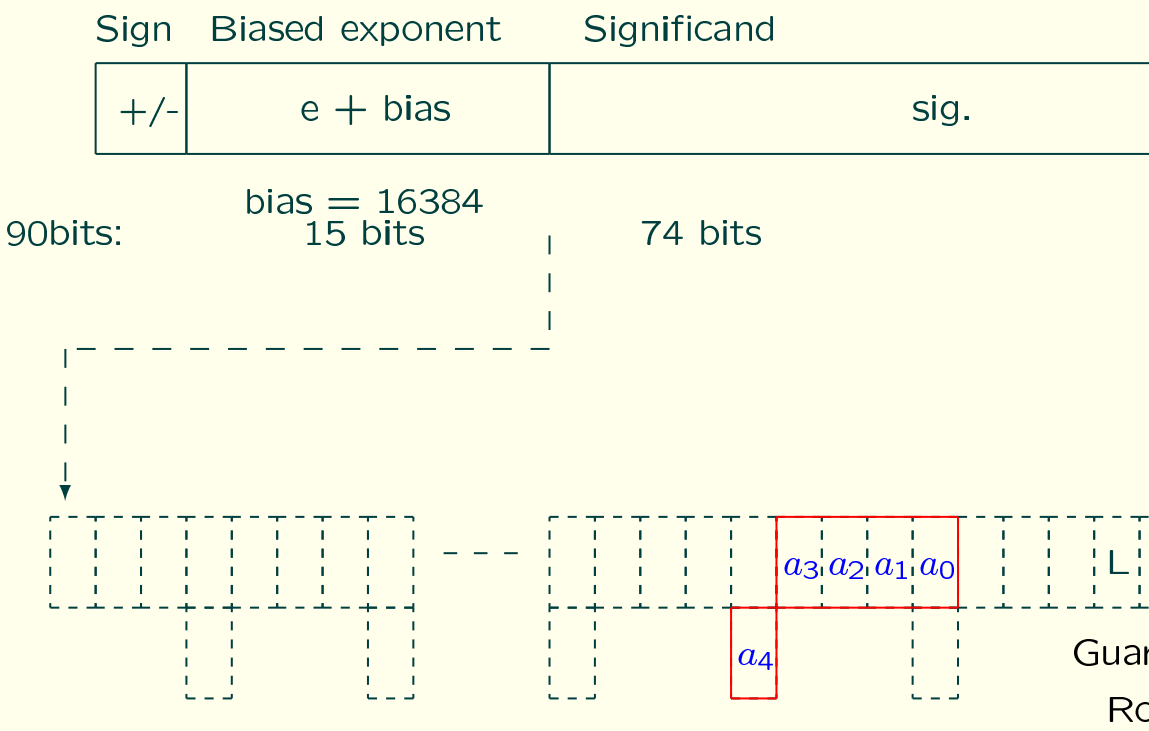
Time delays with redundancy



Time delays with redundancy



Time delays with redundancy



The proposed SD format for floating point n

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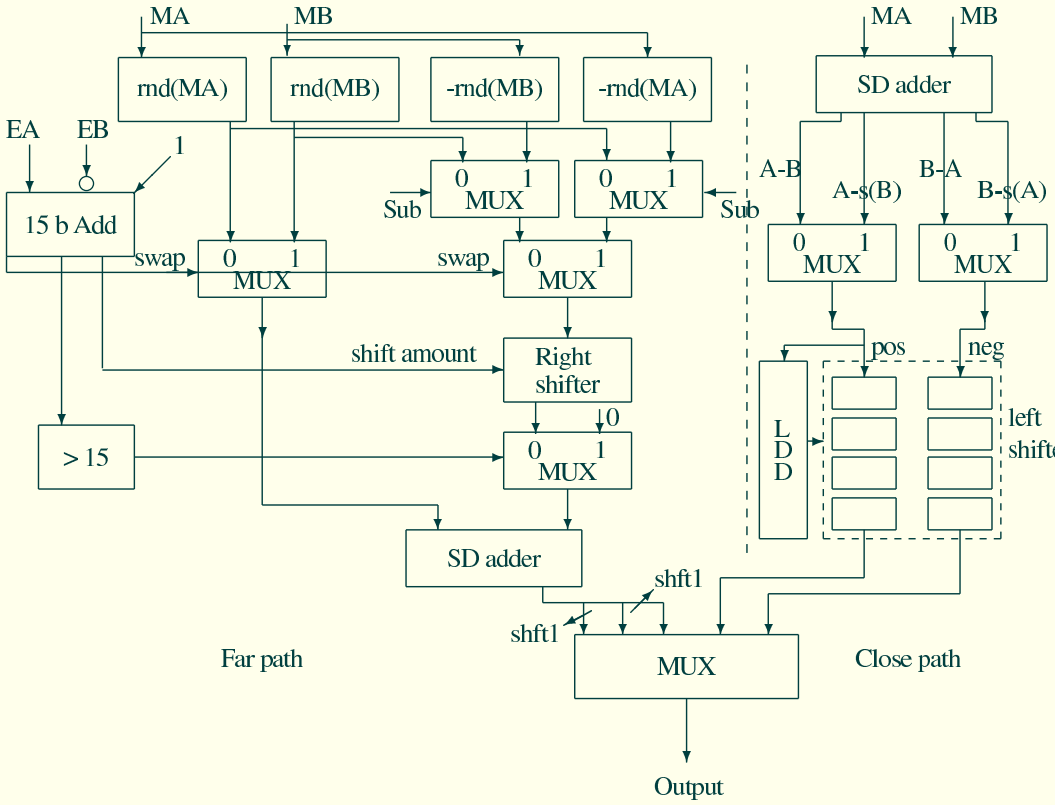


General blocks of the proposed adder (two-path

Background on SD numbers

Ordinary Signed Digit (SD) numbers represent a n
$r > 2$ with digits $x_i \in \{-\alpha, \cdots, -1, 0, 1, \cdots, \alpha\}$ where $\frac{r}{2}$

For example, in decimal where $r = 10$ we have $1\,\overline{8}$ =

Assuming $r = 10$ and $\alpha = 9$ addition goes as

		2	1	$\overline{8}$				2	0	2
	+	7	9	9			+	7	9	9
		9	10	1	$\mid p \mid \geq \alpha$?			9	9	11
1	1	0			c					
		$\overline{1}$	0	1	w					
1	0	0	1		s		1	0	0	1

$$p_i = x_i + y_i \qquad c_i = \begin{cases} -1 & \text{if } p_i \leq -\alpha \\ 1 & \text{if } p_i \geq \alpha \\ 0 & \text{otherwise} \end{cases}$$

$$w_i = x_i + y_i - \beta c_i$$
$$s_i = w_i + c_{i-1}$$

Using as a radix $\beta = 16$ and $\alpha = 15$,

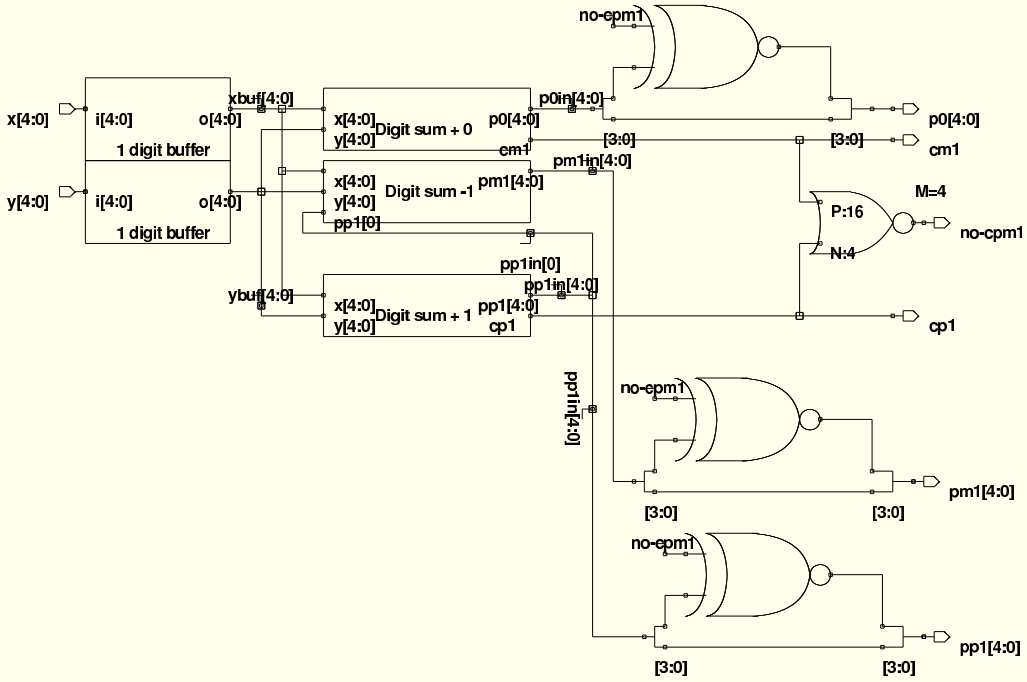
$$\begin{aligned} x_i, y_i, s_i &\in \{-15, \cdots, 15\} \\ p_i &\in \{-30, \cdots, 30\} \end{aligned}$$

In the case of a positive overflow, $x_{i_4} = y_{i_4} = 0$ but p
$w_i = p_i - 16 = p_i - (10000)_2$.

For $c_i = \pm 1$, $w_{i_4} = \overline{p}_{i_4}$

1. $c_{i(1)}$ is set for a positive overflow or a result equa
   of these occur only if $x_{i_4} = y_{i_4} = 0$.
   - The adder calculating $x_i + y_i + 1$ has a posit
   $x_i + y_i \geq 15$

2. $c_{i(-1)}$ is set for a negative overflow or a result eq
   - An output of -15 results if one input is -15 a
   zero or both inputs are negative and their sum eq
   - The inputs being -16 is a don't care condition.

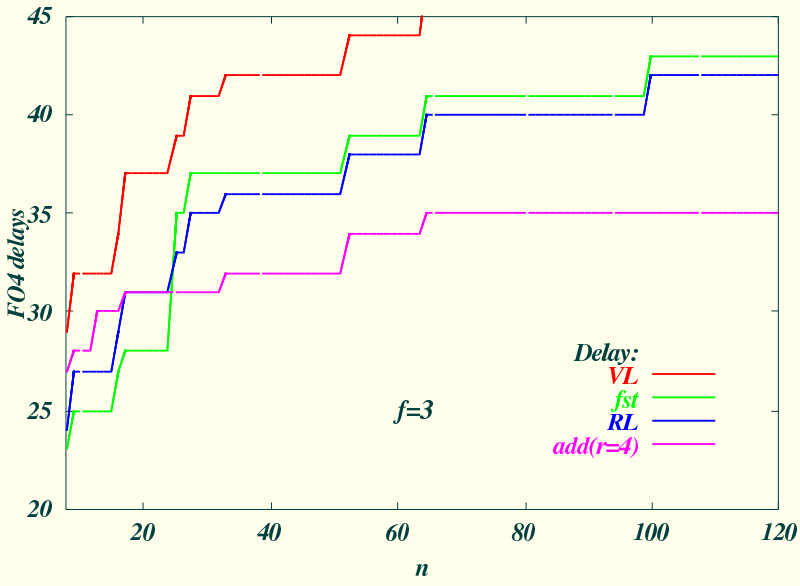


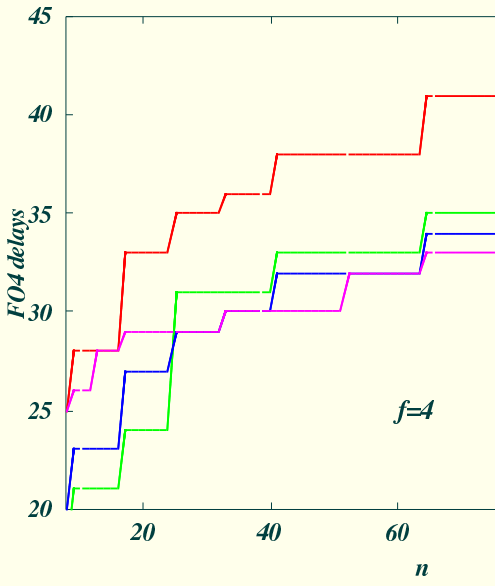
Possible outcomes for one digit

For decimal floating point operations, use $\beta = 10$

$$\begin{aligned} x_i, y_i, s_i &\in \{-9, \cdots, 9\} \\ p_i &\in \{-18, \cdots, 18\} \end{aligned}$$

$$\begin{aligned} c_{i(1)} &= \overline{x}_{i_4}\overline{y}_{i_4}(p_{i_4} + p_{i_3}(p_{i_2} + p_{i_1} + p_{i_0}) \\ c_{i(-1)} &= x_{i_4}y_{i_4}\overline{p}_{i_4} + (x_{i_4} + y_{i_4})p_{i_4}\overline{p}_{i_3} \end{aligned}$$





Complete binary floating point adder compa

Time delay versus significand width for differe

- A scalable CMOS technology was used to design a
  point adder and multiplier at the transistor leve
  $f = 3$ and $r = 4$.

- Both designs perform all the IEEE rounding mod

- Both designs were simulated for functionality at
  using *verilog* and for speed at the transistor level

Circuit statistics and simulation resul

	Floating point adde
number of nodes	46845
NMOS transistors	63589
PMOS transistors	61649
Model delay	$34FO4$
Sim delay($0.6\mu m$)	$14ns$ ($33.35FO4$)
Sim delay($0.3\mu m$)	$6ns$ ($32.40FO4$)

Cost?

		$n = 60$	$n = 80$	n
$r = 4$	width increase(%)	33.3	31.6	
	speed up (%)	10.5	12.5	
$r = 8$	width increase(%)	29.3	21.1	
	speed up (%)	7.9	10	

Floating point adder trade off when $f =$

Conclusions and Contributions

- A new internal format based on SD numbers and t
  ing floating point unit adder are presented

- The SD adder is adapted to perform decimal add

- Through analytical modeling and transistor simul
  posed designs perform better than the conventior
  double precision numbers.