Characterization of a coaxial mid-gap SB CNTFET inverter

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1. Introduction

Many research groups attempt to extend Moore's law for digital circuits beyond the expected end of the CMOS scaling by proposing alternate devices. Carbon NanoTube FETs, CNTFETs, are among the most promising devices. In this paper, we investigate the performance of digital inverter gates based on mid-gap Schottky Barrier CNTFET with coaxial structure. This structure is the most suitable CNT structure for future 3D integration.

2. Simulations and Results

We simulate the mid-gap SB CNTFET using publicly available models [1, 2]. The inset of Fig. 1 shows the structure of the device and the main figure shows its ambipolar characteristics. The minimum current I_{min} occurs at $V_{gs}= V_{ds}/2$ leading to a bad performance for the inverters. The performance is greatly enhanced by shifting the characteristics along the V_{gs} axis to align I_{min} at $V_{gs}=0$. This alignment is done in reality using a suitable gate material to adjust the flat band voltage to $V_{fb} = V_{dd}/2$.

The tabulated I-V data of a single device is used to analyze the inverter circuit. We use a multi-stage fan-out of 4 inverter chain to simulate the dynamic performance of a loaded inverter. Each inverter drives a pure capacitive load since we neglect the gate tunneling current (in the order of pA for ultra thin high k dielectric transistors [3]). The total capacitance [4] of each transistor is $C_g^{-1} = C_{es}^{-1} + (4C_Q)^{-1}$ where C_Q is the quantum capacitance and C_{es} the electrostatic capacitance including the parasitic capacitance calculated by FASTCAP [5]. We also neglect the metal contacts resistance since the minimum channel resistance is at best 6.5 KΩ and only contacts with resistance 10 KΩ or higher affect the performance [6].

Fig. 2 shows the Voltage transfer Characteristic (VTC) for two inverters based on two different device type ($V_{fb}=0$ and $V_{fb}=V_{dd}/2$) at $V_{dd}=0.5V$. Although the inverter gain in the case of $V_{fb}=0$ is larger, the voltage swing (Fig. 3) and both V_{OH} and V_{OL} (Fig. 4) are better for $V_{fb}=V_{dd}/2$. Fig. 5 shows the output of stages 3 and 4 of the inverter chain for the two types at $V_{dd}=0.5$ and an input frequency of 10GHz. The logic is lost completely after the 4^{th} stage for the case of $V_{fb}=0$. Fig. 6 shows the chip static power density assuming 10^9 inverters/cm^2 in future technologies. The inverter with $V_{fb}=0$ transistors has an unacceptable static power. Assuming that 20% of the circuit is switching in any cycle, the dynamic power at 10GHz is noticeably less than static power for both types of inverters.

3. Conclusion

The midgap SB CNTFET with $V_{fb}=0$ is easier to fabricate and produces identical n and p transistors but it does not satisfy any other requirements for future digital applications. On the other hand, the DC and transient performance of $V_{fb}=V_{dd}/2$ transistors are better but the fabrication is more difficult and uses different materials for the gate of the n and p types.

For the power consumption, midgap SB CNTFET with $V_{fb}=V_{dd}/2$ satisfies the requirements for low power applications at supply voltage $V_{dd}=0.5V$ expected in the year 2020, taking into consideration the good heat conduction ability of CNTs. The large static to dynamic power ratio is a weak point of the various CNT devices proposed in the literature including ours. We are still looking for better device structures to use the great characteristics of CNTs and find a replacement to CMOS.

References

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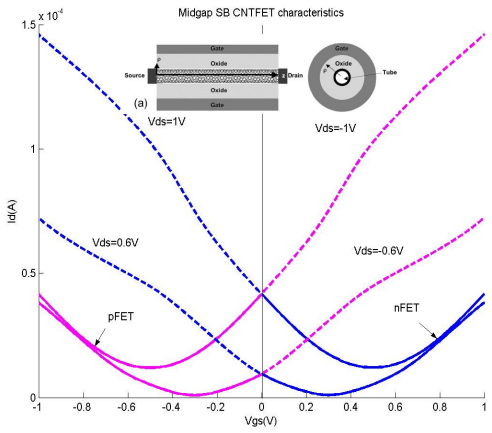

Fig. 1 I-V characteristics of our midgap SB CNTFET with V_{fb}=0.The inset shows the schematic of the transistor.

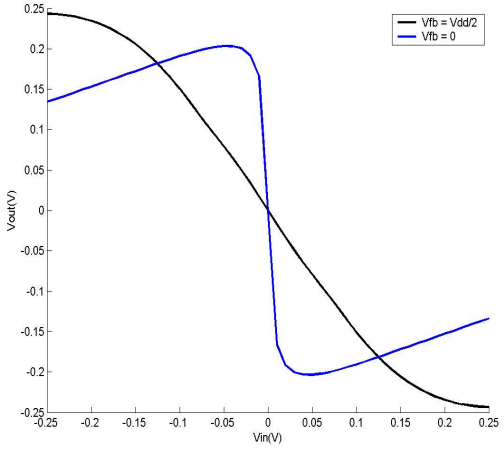

Fig. 2 VTC of the two types of inverters.

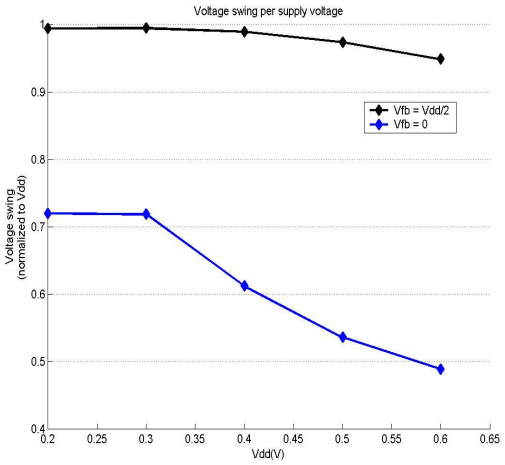

Fig. 3 The voltage swing of the two inverters normalized to supply voltage.

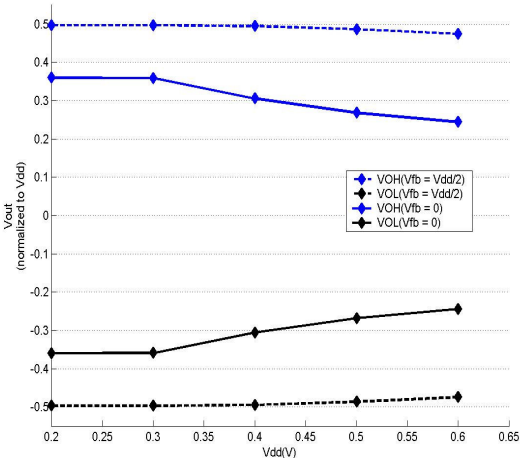

Fig. 4 V_{OH} and V_{OL} of the two inverters normalized to supply voltage.

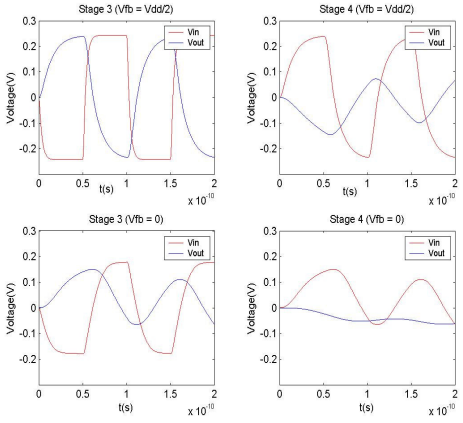

Fig. 5 The input and output voltage at stages 3 and 4 of the inverter chains.

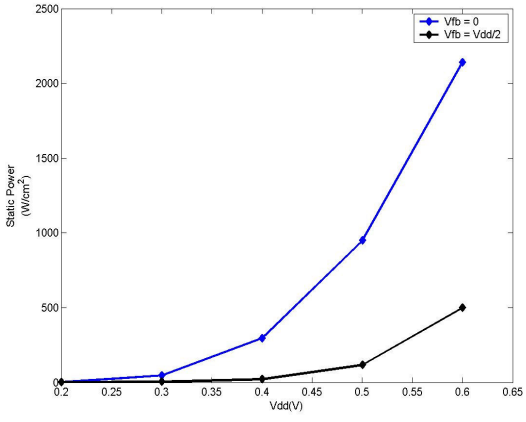

Fig. 6 Static power density of the two inverter types.