Analysis of a single-electron decimal adder

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In this letter, a decimal adder using single electron transistors as a building block is presented. The design is described and the equivalent circuit is extracted, from which the dc performance of the adder is derived. This simple analytical approach is found to be in good agreement with numerical simulation. A detailed sensitivity analysis is performed where the effects of temperature, capacitance, conductance, and background-charge variations are analyzed and the attendant change in device performance is described. This adder needs a number of wires four times less than binary adders and hence alleviates the interconnections problem present in high density circuits. © *1997 American Institute of Physics.* [S0003-6951(97)00719-5]

In the past few years, several proposals were suggested for performing logic and memory applications using single electronics or quantum dots. Some of these involved using the single electron transistor (SET) as a replacement for the standard field-effect transistor,[1,2] while others proposed using each electron to represent a single bit, in what is known as the single electron logic (SEL).[1,3] Others came up with even more radical ideas about the architecture and signal coupling between different parts of the circuit that should be used.[4–7] This was targeted to solve the wiring crisis and high power dissipation present in the previous proposals. Another possible approach to solve the interconnections problem is presented here by the use of decimal multivalued logic. Only one wire is needed to represent a digit from 0 to 9, whereas if using binary adders four wires are needed.

SETs have an inherent ability to perform multivalued operations due to their ability to ''count'' the charges trapped in a quantum dot and because the quantization levels for the charge are quite clear. Each step represents the addition of an extra electron to the dot. The device proposed here is a variation of the SET found in the literature, but instead of having one gate to control the charge tunneling, two gates are assumed. If the voltage between the drain and source is kept constant, the charge in the dot will be proportional to the sum of the two gate voltages which are considered as the inputs here.

A schematic top view of the proposed device is shown in Fig. 1(a). It can be achieved using scanning tunnel microscope (STM)/atomic force microscope (AFM) nano-oxidation[8] or any other nanofabrication technique. Figure 1(b) shows the equivalent circuit of the intrinsic device. The sensing of the resulting number of electrons is performed by coupling the device to an electrometer which converts the value of the charge into a corresponding voltage[9] [Fig. 1(c)]. The analytical analysis of the intrinsic circuit follows the same steps used for other proposals,[10] i.e., drain and source voltages are assumed to be zero and only the effect of the gates is considered.

Positive voltage on the gates induces negative charges in the dot, while the dot voltage induces positive charges in it. The difference, which represents the charge of electrons trapped, is $-nq$, where n is the number of electrons in the dot and q the charge of a single electron. The energy of the circuit, U, may be written in terms of the charges on the capacitors C_{g_1}, C_{g_2}, C_d, C_s and then transformed to the following form,[10]

$$U=[(qn)^2-2qnC_{g_1}V_{g_1}-2qnC_{g_2}V_{g_2}+2C_{g_1}C_{g_2}V_{g_1}V_{g_2}-C_{g_1}(C_{g_2}+C_s+C_d)V_{g_1}^2-C_{g_2}(C_{g_1}+C_s+C_d)V_{g_2}^2]/(2C_{tt}), \tag{1}$$

where $C_{tt}=C_{g_1}+C_{g_2}+C_s+C_d$. This form is preferred because it gives the energy in terms of the external inputs and the measured quantity n. The tunneling event occurs only when it is favorable from the energy point of view, i.e., when it causes a minimization of U. By differentiating Eq. (1) and assuming symmetric gate capacitances ($C_{g_1}=C_{g_2}=C_g$), the increment in the sum of gate voltages required to trap an extra electron is found to be,

$$\Delta V\equiv\Delta(V_{g_1}+V_{g_2})=\frac{q}{C_g}. \tag{2}$$

This indicates that ΔV is constant, independent of the absolute voltage present on the gates, and that it is a step representing the sum of the two inputs.

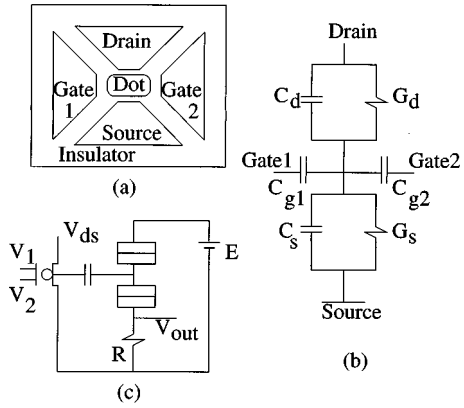

FIG. 1. (a) Schematic top view of the dual-gate SET; (b) equivalent circuit used in the simulation; and (c) dual-gate SET capacitively coupled to an electrometer to sense the charge.

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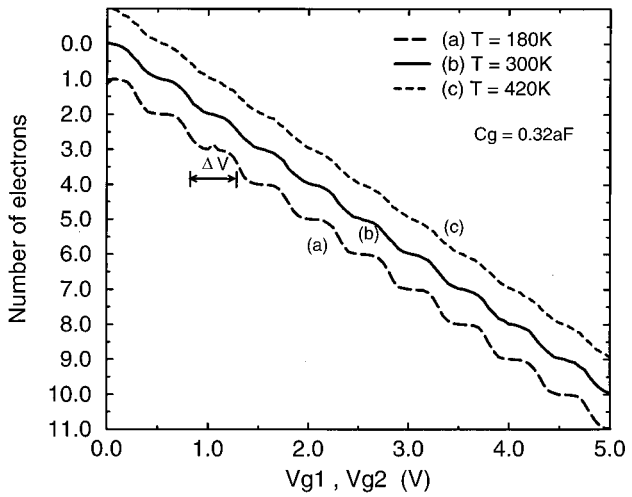

FIG. 2. Temperature effect on the adder performance. Curve (a) is shifted down by 1, and curve (c) is shifted up by one for clarity.

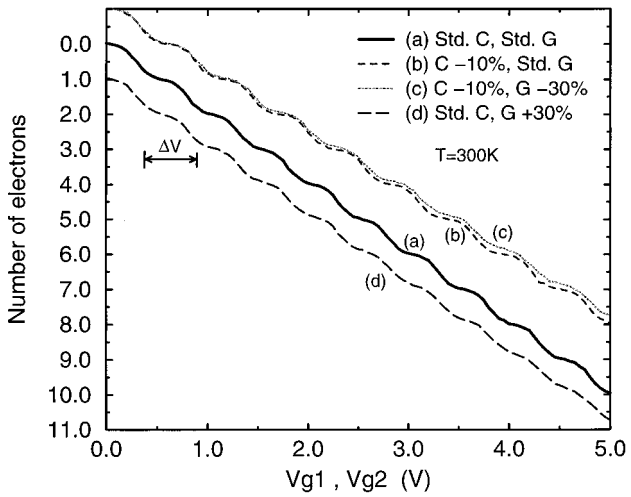

FIG. 3. Effect of capacitance and conductance variation (the values corresponding to std. C are: $C_g=0.32\ aF$, $C_s=C_d=0.08\ aF$, and that corresponding to std. G is $G=1\ \mu$s). All capacitances are scaled together. Curves (b) and (c) are shifted up by 1, and curve (d) is shifted down by 1 and for clarity is 15 nm thick in all cases.

We have performed numerical simulation of the device performance,[11] assuming $C_g=0.32\ aF$ and $C_s=C_d=0.25\ C_g$. The two gate voltages are swept together from 0 to 5 V resulting in tunneling occurring at steps of nearly 0.5 V (Fig. 2). This is in agreement with the analytical result of Eq. (2). If the tunnel resistance is assumed to be 1 M Ω ($\gg h/q^2$), the time constant of the device is $\tau=RC_{tt}=0.8$ ps. The device itself is quite fast and—depending on its loading in a real circuit—high speed operation can be achieved.

The sensitivity of the adder to temperature, capacitance, and conductance variations has been also investigated. Figure 2 shows the effect of temperature increase. Although with high temperature the steps seem to wash out, the output is still the correct value of the addition of the inputs. However, signal restoration may become a problem because of reduction in noise margins.

Fabrication tolerances can cause the thickness of the insulator between the different electrodes to vary, which leads to capacitance variation. The sensitivity of ΔV to the gate capacitance is calculated from Eq. (2) to be $S_{C_g}^{\Delta V}\equiv(\partial\Delta V/\Delta V)/(\partial C_g/C_g)=-1$. This indicates that the circuit is quite sensitive to the capacitance value. Figure 3 shows the numerical calculation result when all the capacitances are reduced by 10% [compare curves (a) and (b)]. The predicted sensitivity of ΔV is clearly observable, manifested in each plateau increasing by 10%. This error, however, is cumulative such that when $V_{g_1}+V_{g_2}=10$ the number of electrons in the dot is only nine.

We have also examined the effect of varying the tunneling conductance which is exponentially dependent on the insulator barrier height and thickness.[12] Comparing curves (b) and (c) in Fig. 3, where capacitances are equal but conductances differ by 30%, it is seen that the conductance decrease has nearly no effect. On the other hand, comparing curves (a) and (d) in Fig. 3, a conductance increase by 30% causes the steps to gradually smear out. This may be attributed to increasing the cotunneling probability, which destroys the coulomb blockade. It is important to note that, in practice, the capacitance and the conductance change in the same direction with the insulator thickness variation [curve (c)].

In addition to parameter variations, fabrication tolerances may induce background charge on the dot. This has a detrimental effect on the functionality of the single-island device by adding an offset to the I–V characteristics as shown in Fig. 4, where four random charge offsets are assumed. The use of multiple islands is known to suppress the cotunneling effect and the offset charges present.[13] Assuming five islands having a random offset charge distribution results in a much more robust device since the effect of the different charges on the islands averages out to nearly zero (Fig. 4).

The presented decimal adder has a huge area advantage when compared to a four bit complementary metal-oxide semiconductor (CMOS) adder capable of performing the

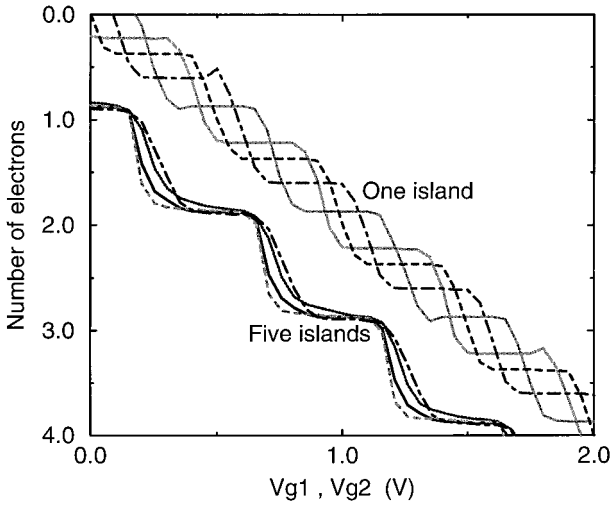

FIG. 4. Effect of background charge variation. The charges are chosen randomly with a normal distribution (mean=0, standard deviation=0.2q). The ''five islands'' family of curves is shifted down by 1 for clarity.

same function. This is mainly due to the fact that here it is a single device (in addition to another device and a resistor needed for charge sensing) which performs the decimal addition. In contrast, about 60 transistors would be needed to build a decimal adder (based on four 1-bit binary adders). This translates into more than an order of magnitude reduction in total intrinsic device area. Since a significant percentage of the area and time delay are attributed to the wiring of the devices, the reduction in the number of wires results in a considerable advantage. It is important to note, however, that the above evaluation is based on a dc analysis and that speed comparison including loading effects, which is subject of further study, has been ignored.

In conclusion, we have presented a decimal adder based on a single electron device where the number of active devices and wires are significantly reduced compared to conventional CMOS adders. It was found that sensitivity to parameter variations is a clear shortcoming of the decimal adder, since small changes in the design parameters and the attendant change in capacitances, conductances, and offset charges have dramatic effects on the functionality of the adder. The use of multiple islands instead of only one, however, has the potential of averaging out such fluctuations.

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