The SNAP Project:
Towards Sub-Nanosecond Arithmetic

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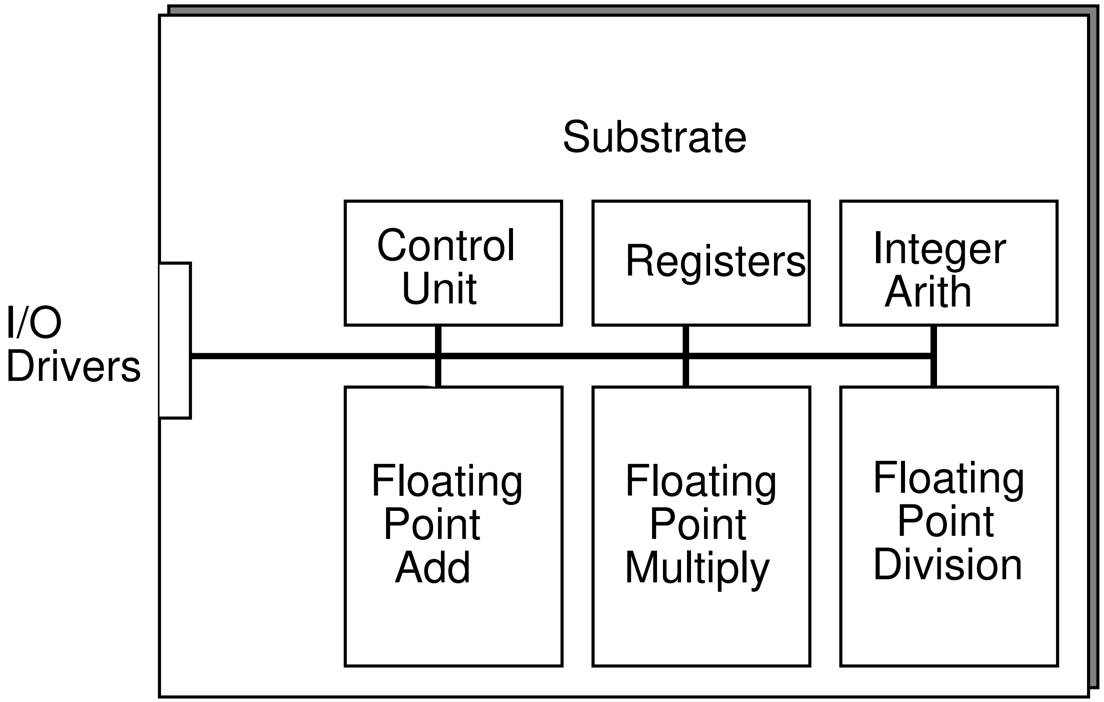
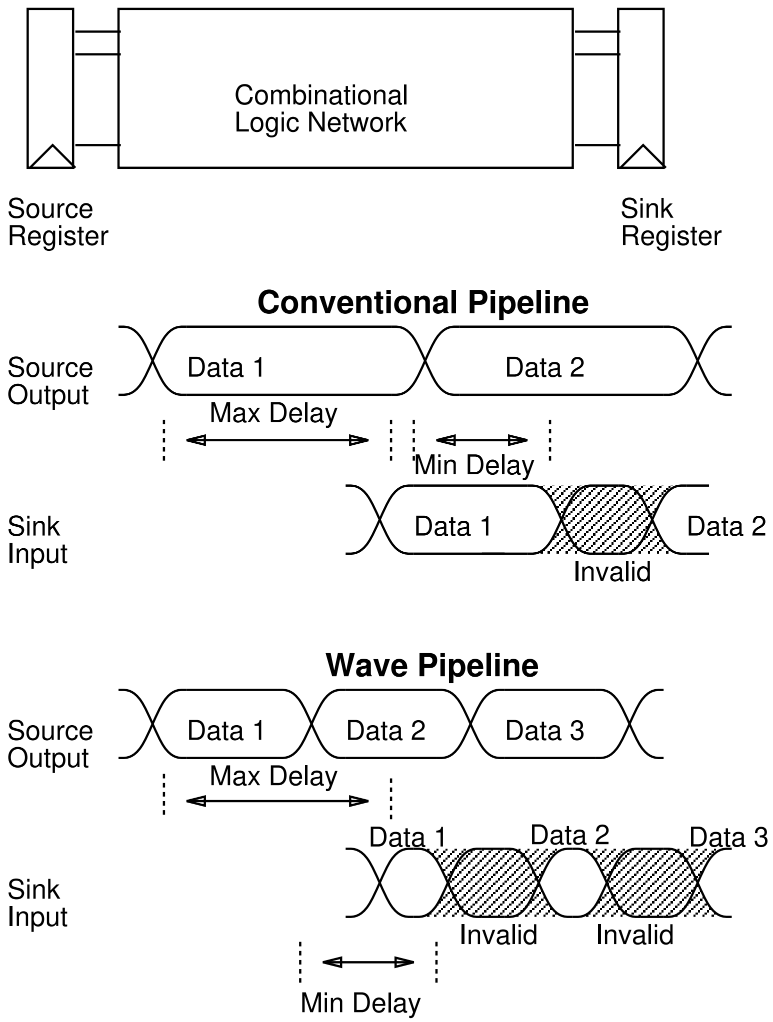
SNAP PROCESSOR



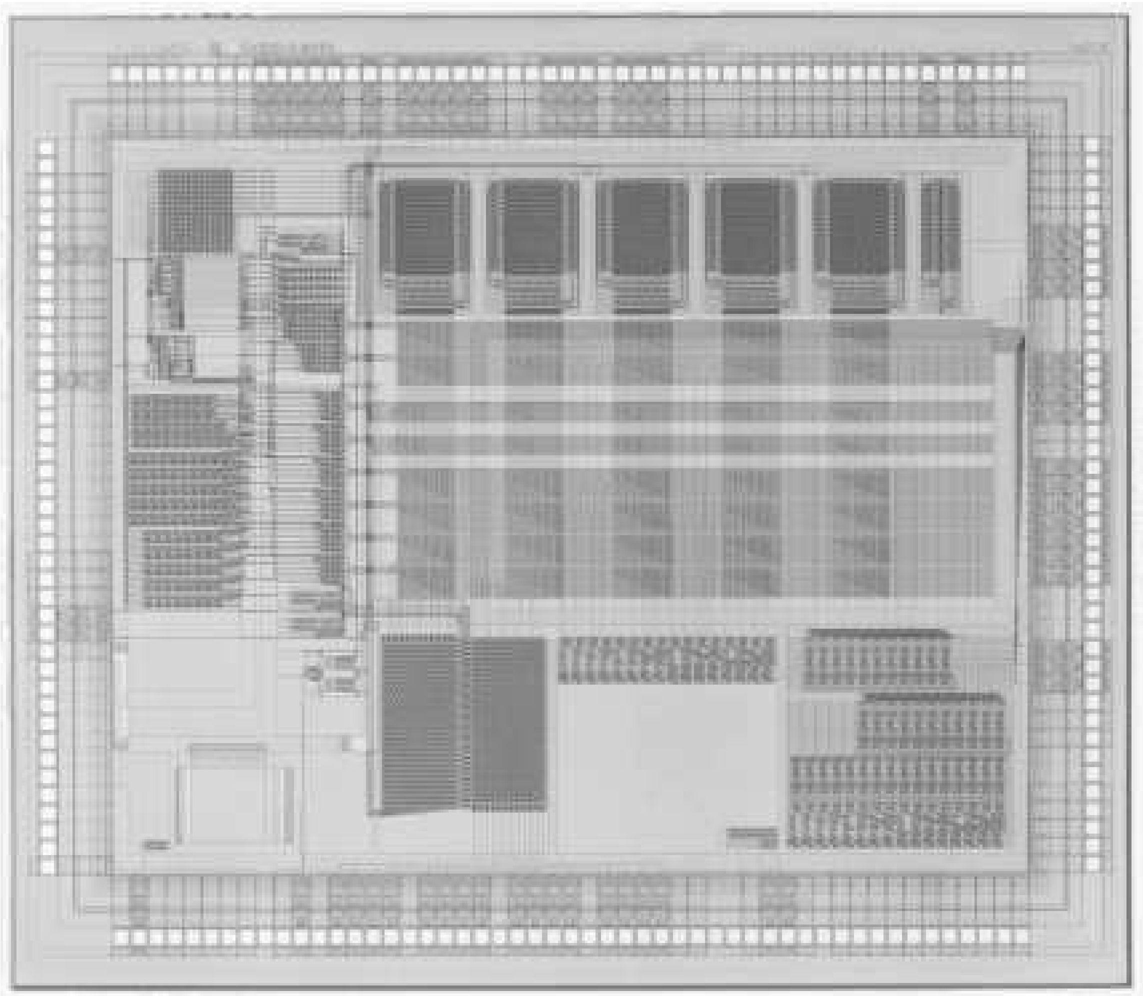
SNAP DIE FAB STATUS

Die	Company	Technology	Status	Result
Integer Adder	Signetics	ECL	FT	2ns 32b integer
FP adder	HP Research	CMOS	IT	15ns
Multiplier slice	Signetics	BiCMOS	FT	< 10ns
Multiplier slice	Signetics	BICMOS	FT	< 7ns
FP multiplier	Sun	ECL	IT	5ns
W.p. multiplier slice	Signetics	ECL	FT	3.8ns
W.p. multiplier 16x16b	NSF	CMOS	FT	3.3ns
W.p. vector unit	NSF	CMOS	FT	3.3ns
Divider	-	CMOS	NYS	Under study

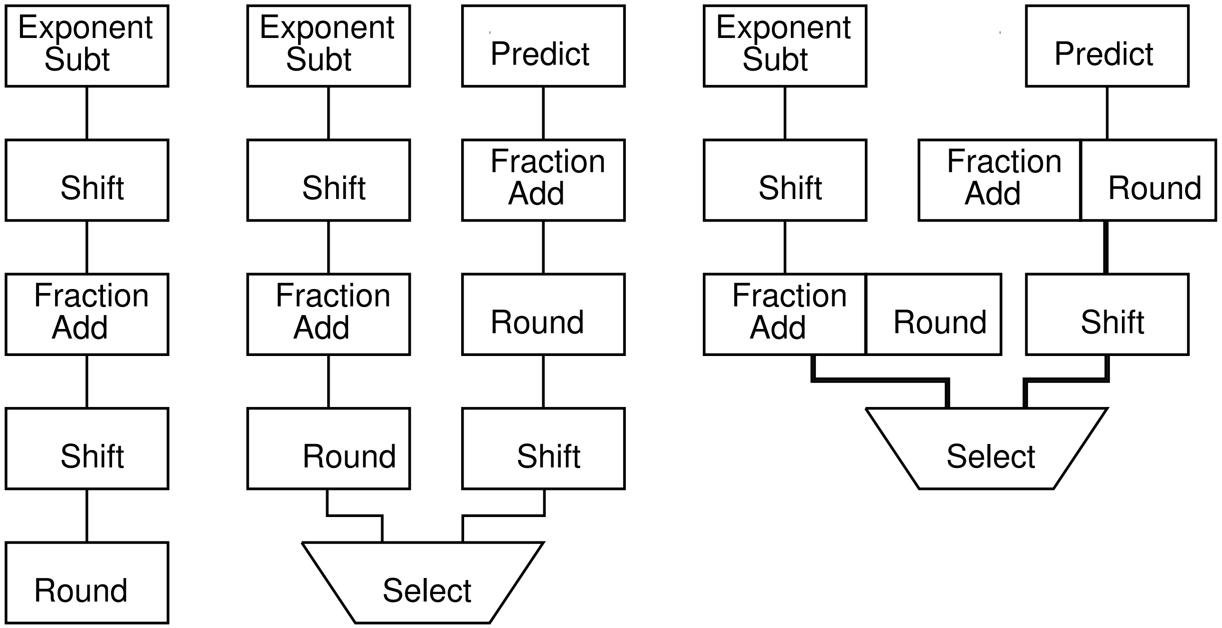
CONVENTIONAL AND WAVE PIPELINE TIMING



WAVE PIPELINED VECTOR UNIT

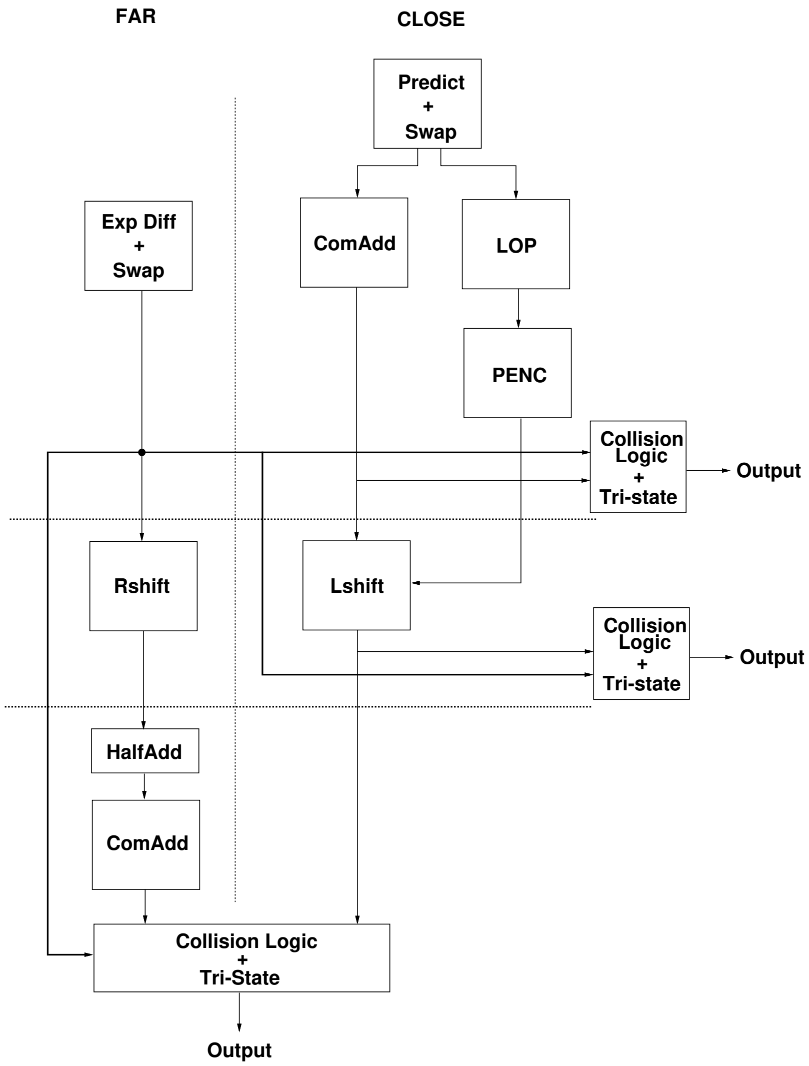


FLOATING POINT ADDITION ALGORITHMS



(a) Traditional **(b) Two Path** **(c) SNAP**

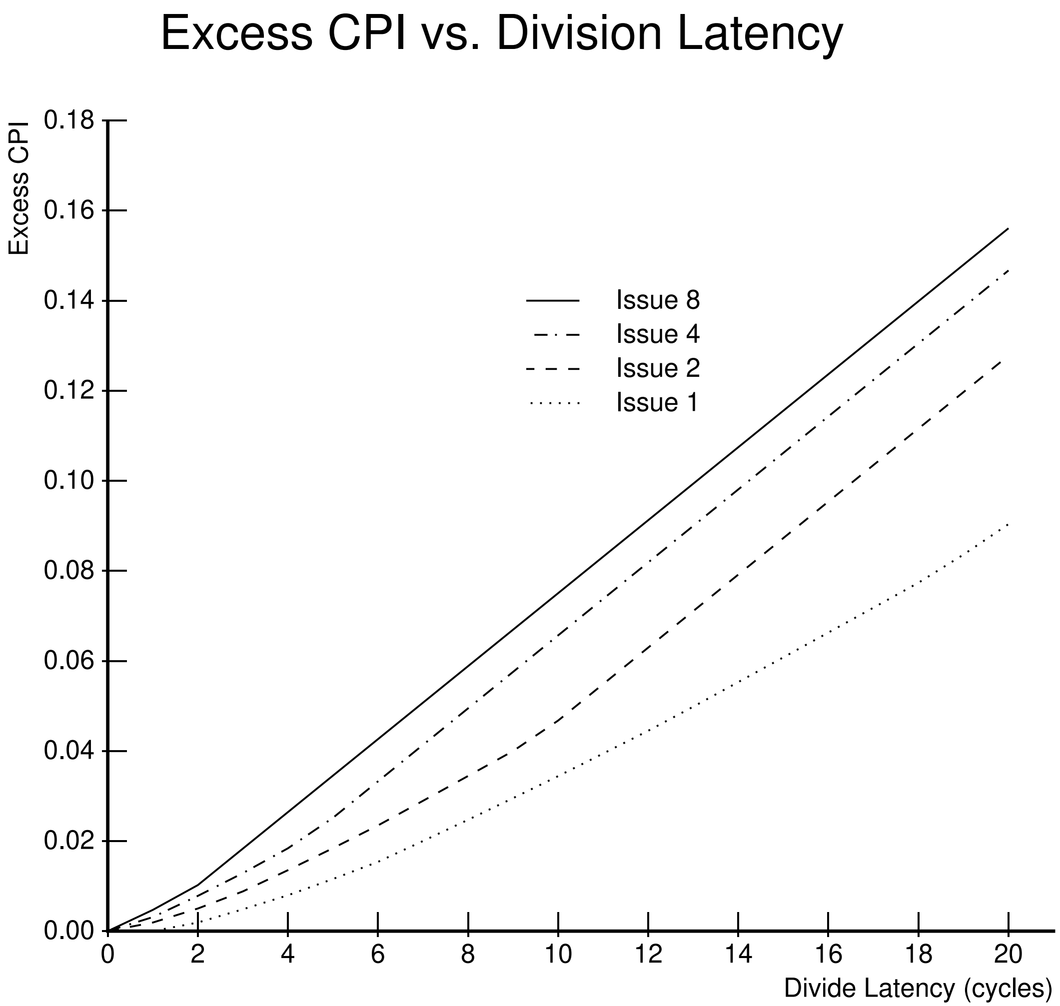
VARIABLE LATENCY FLOATING POINT ADDER



SYSTEM LEVEL STUDY OF DIVISION LATENCY

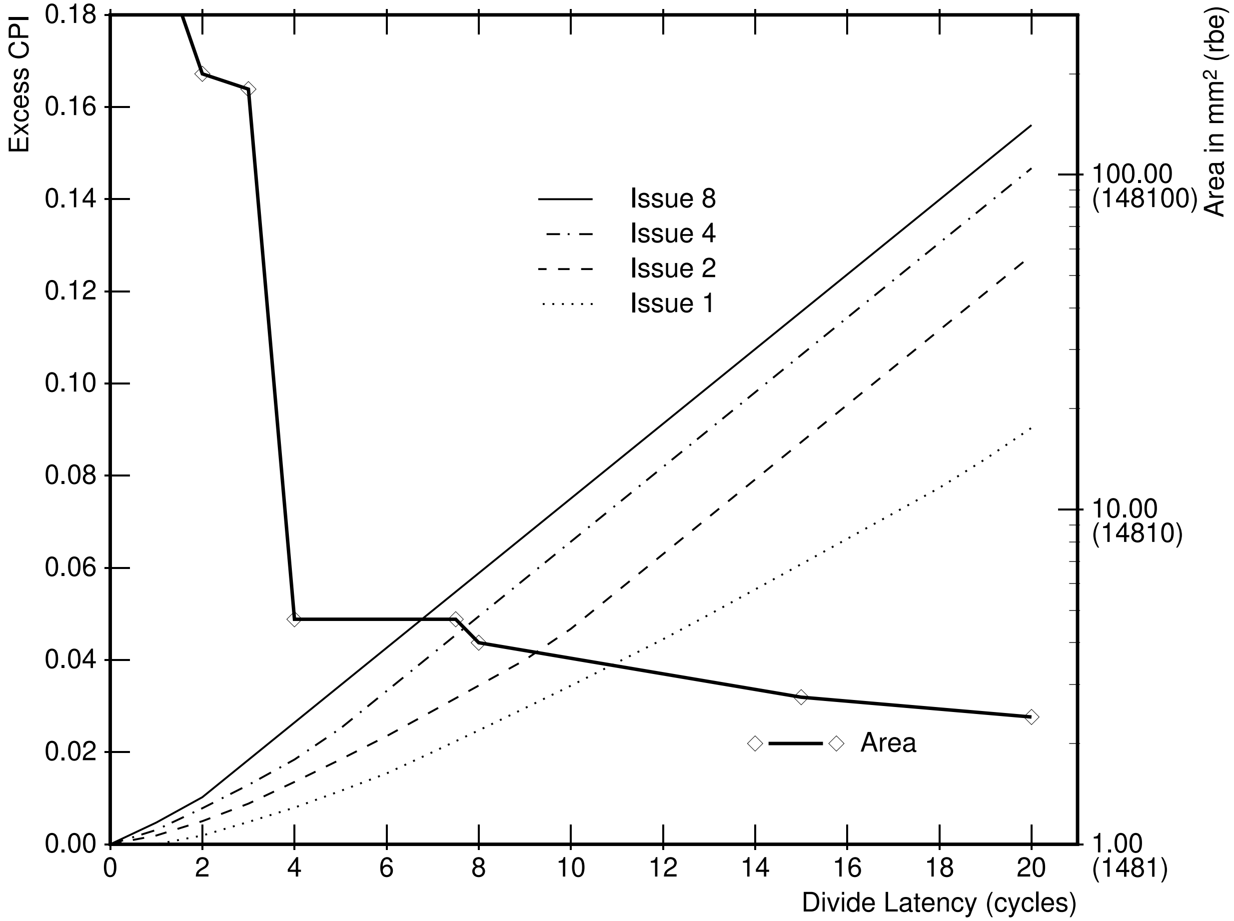
- Profile SPECfp92 benchmark suite
  - Compile sources at 3 different optimization levels on DECstation 5000
  - Instrument binary using pixie
  - Execute new binary on regular input data set
- Investigate several design issues:
  - **System performance vs division latency**
  - **Compiler scheduling ability to improve division performance**
  - **Effects of multiple issue**

SYSTEM PERFORMANCE



PERFORMANCE/AREA

Excess CPI and Normalized Area vs. Division Latency

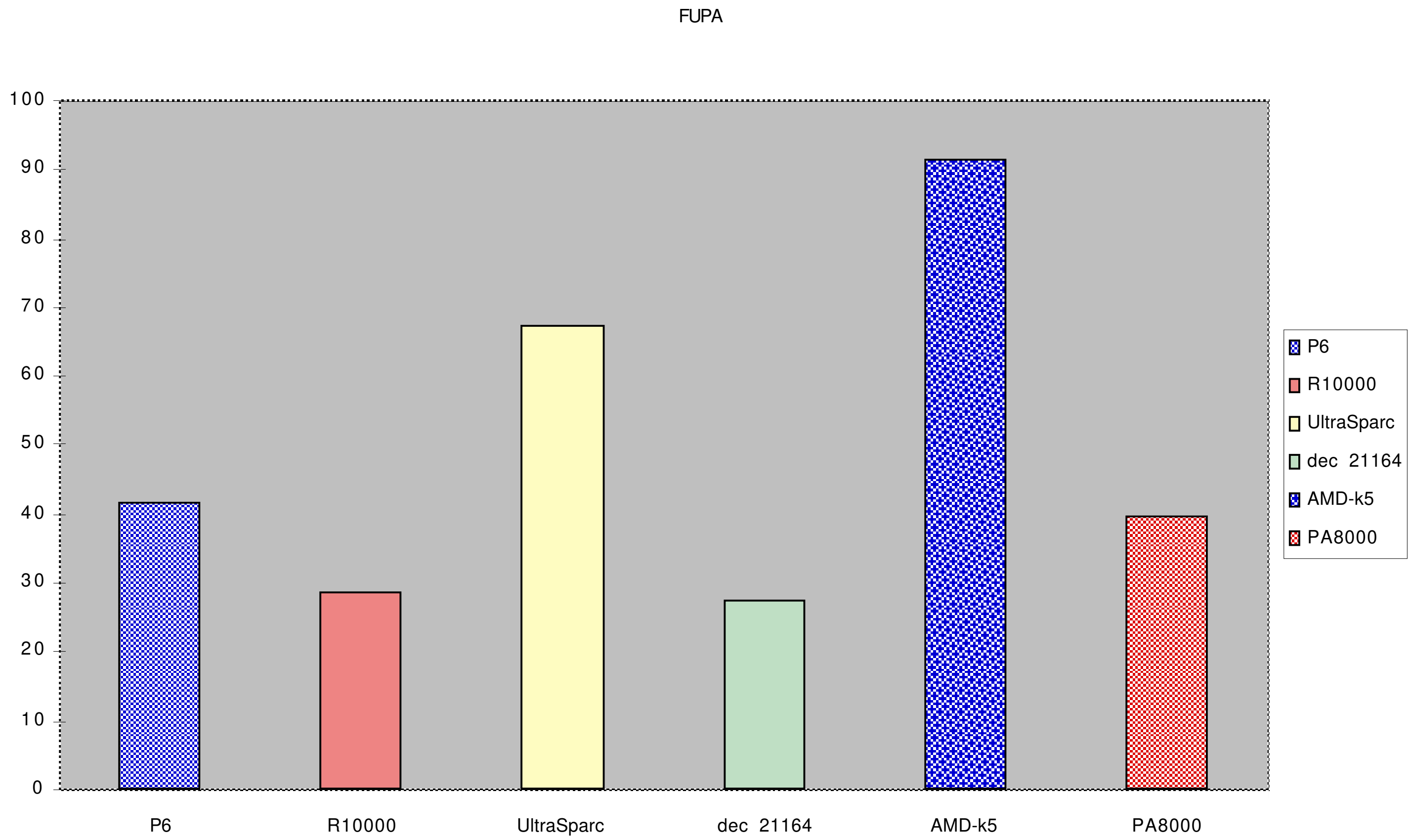


WHAT IS FUPA

- A metric for optimizing and comparing floating-point unit implementations

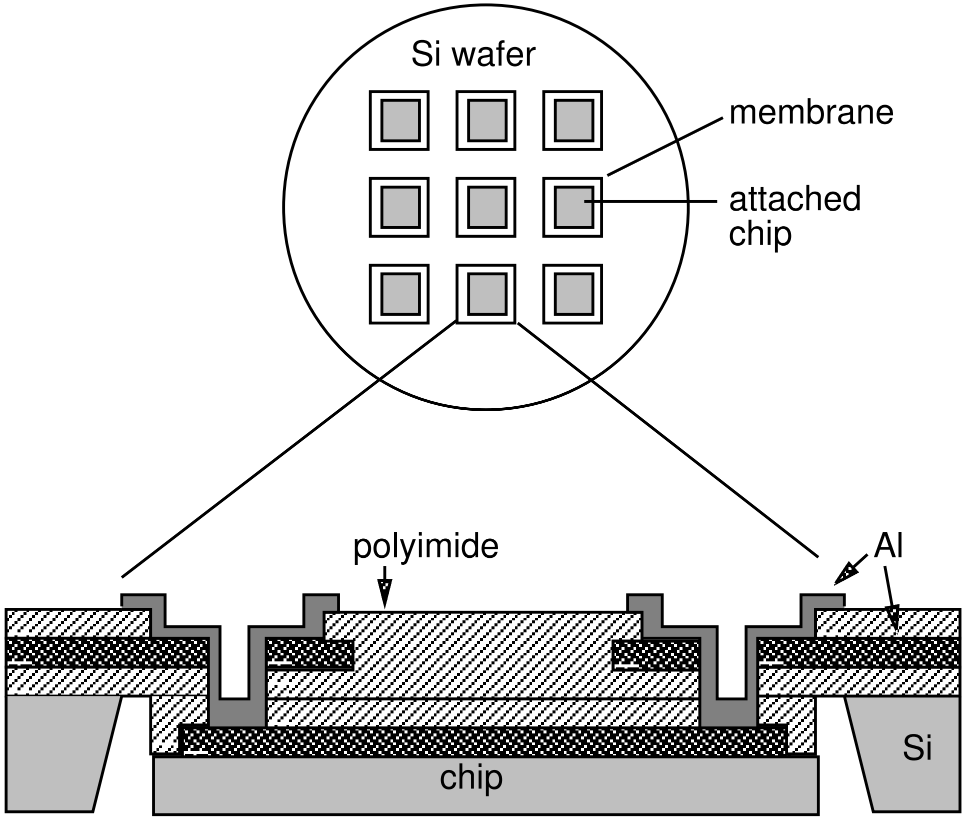
- Comprises four aspects:
  - Latency
  - Cost
  - Technology
  - Profiles of target applications

FUPA



FUPA
100
90
80
70
60
50
40
30
20
10
0
P6
R10000
UltraSparc
dec 21164
AMD-k5
PA8000
P6
R10000
UltraSparc
dec 21164
AMD-k5
PA8000

MEMBRANE MULTI-CHIP MODULE



WORLD-WIDE-WEB SITE

For more information:

Stanford Architecture and Arithmetic Group

http://umunhum.stanford.edu

On-line Processor Design Tools

http://umunhum.stanford.edu/tools